LECTURE NOTES ON

VLSI AND EMBEDDED SYSTEM

5th SEMESTER ETC

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Very large Scale Integrated Circuits (VLSI)

Historical perspective of VLSI Circuit:-

→ There are many invations in 20th Century,
Ex:- Computers, Nuclear power generation.
Airplanes etc.

→ All this things has to be controlled by electronics.

What is electronics?

Ans → To use electrons, electronic circuits etc IC.
Ex: without IC mobilephone can not be made.

→ In 1958 radio → TV made of vacumetube.

→ Electronics is the most important invations in the 20th Century.

→ Now a days vacum tubes is replaced by VLSI.

→ First computers is made up of huge number of vaccume tubes in 1946 which has bigger size, need, huge power, short lifetime flamable, costly.

→ In 1947, first point contact bipolar transistors invented.
Ex:- Ge semiconductors (Bardeen, Brattain)

→ In 1948 first junction bypolare transistor was invented.
(William Shockley)

→ In 1948 first Integrated Circuit was invented. (Jack Kilby

→ In 1959 first planal integrated circuit was invented.
(Robert Noyce)

→ In 1960 first MOS transistor was invented (Kahng and Atalla)

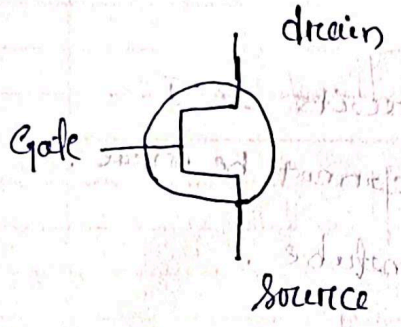
→ In 1964 transistors just started

→ In 2012 all the things is controled by Silicon integrated circuit.

Classification of CMOS (Complementary metal oxide Silicon)

→ CMOS consist of (1) NMOS
(2) PMOS

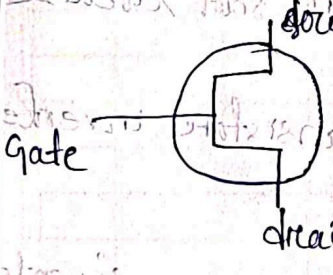
NMOS



If gate = 0 ⇒ off (Drain to Source is open circuit)

If gate = 1 ⇒ on (Drain to Source is shorted circuit)

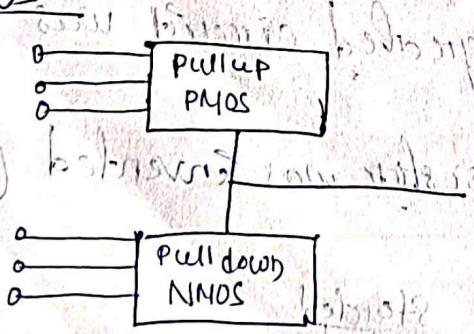
PMOS



If gate = 0 ⇒ on (Source to Drain is short circuit)

If gate = 1 ⇒ off (Source to Drain is open circuit)

CMOS



PMOS transistors pass logic high.

NMOS transistor pass logic low.

Basic rules of ~~digi~~ design a circuit

(•) operation / AND gate operation

PMOS (parallel)

NMOS (series)

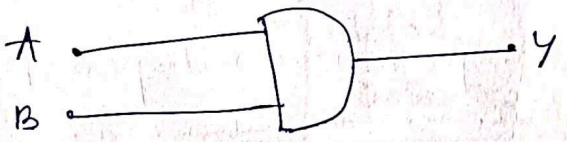
(+) operation / OR gate operation

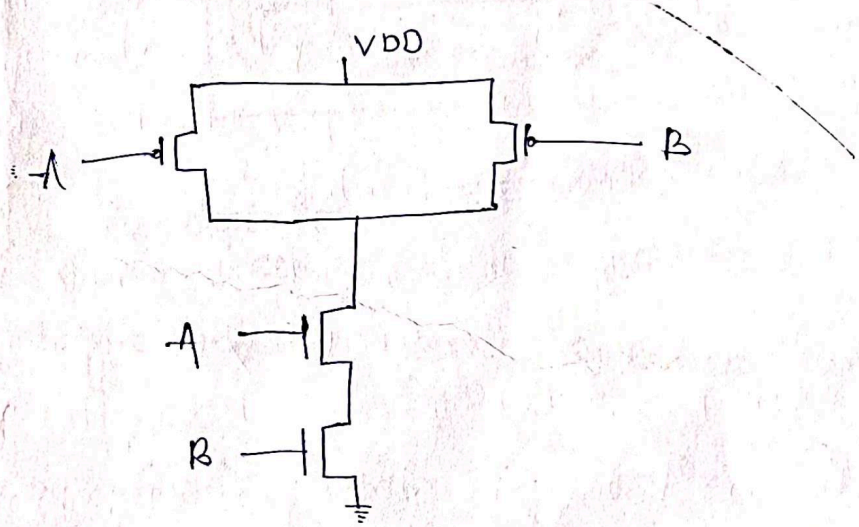
PMOS (series)

Nmos (parallel)

CMOS NAND gate operation

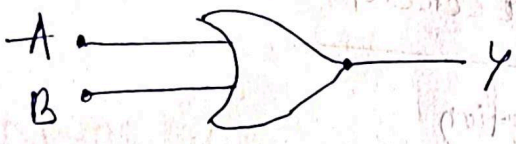
equation = $\overline{A \cdot B}$

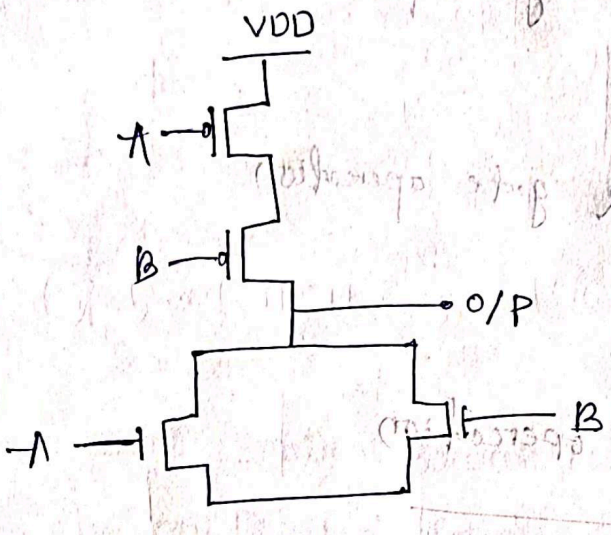




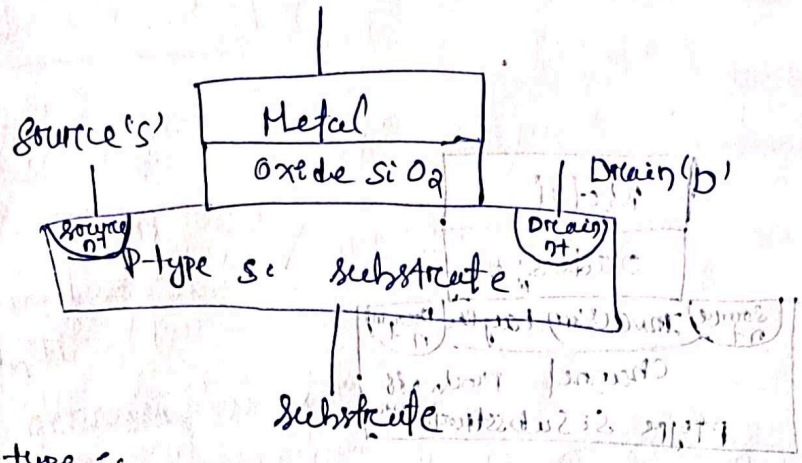
CMOS NOR gate operation /(+) operation

Equation = $(\overline{A+B})$



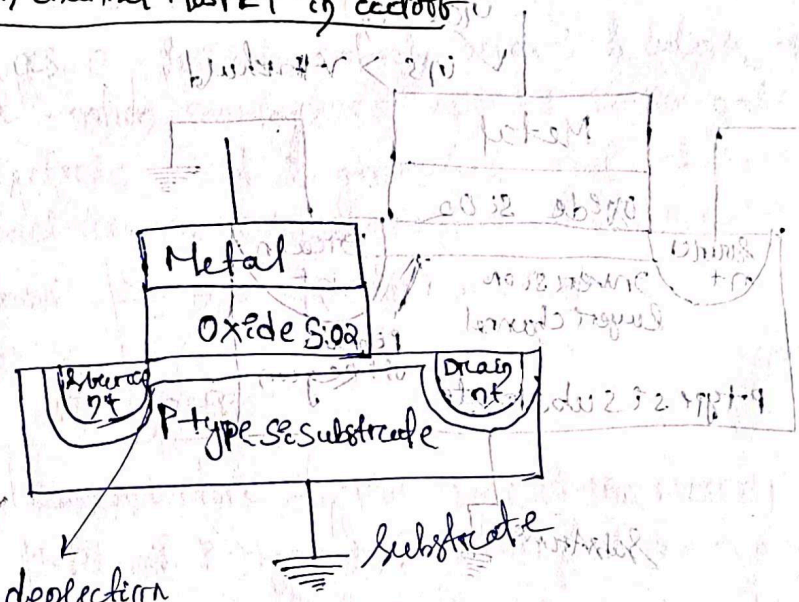


Structure of n channel MOSFET :-

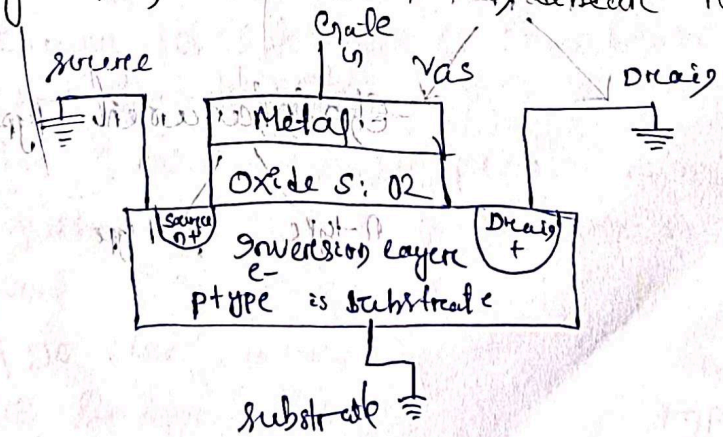


P-type is
The base of the MOSFET

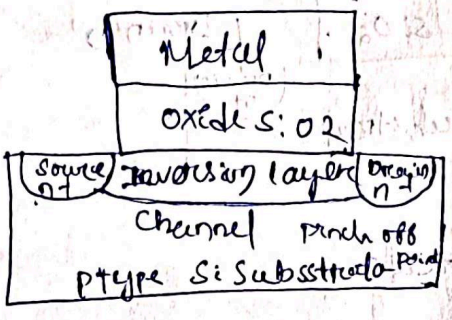
Working of n channel MOSFET in cutoff region :



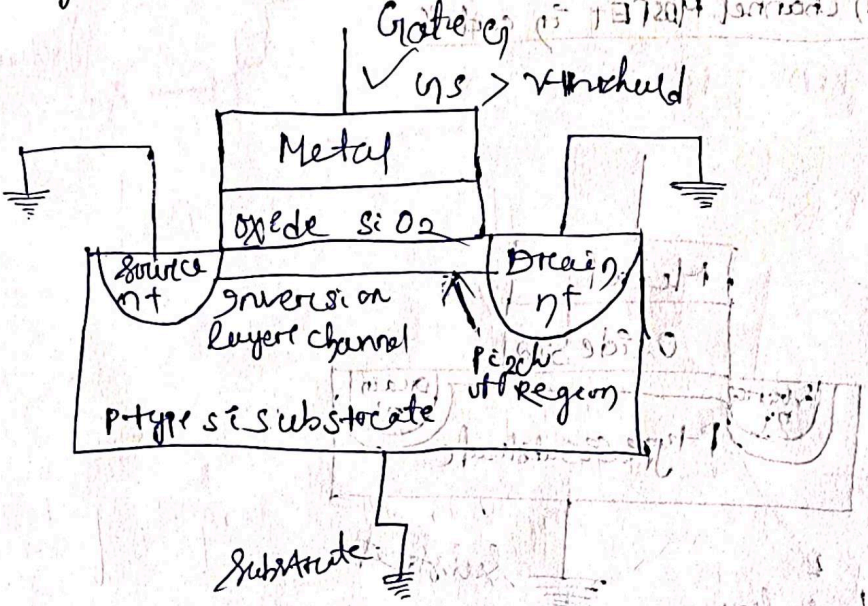
Working of n channel MOSFET in linear region :-



Working of n channel MOSFET - Threshold of inversion region :-



Working of n channel MOSFET in Saturation



Voltage Drop across pinch off Region will be $V_{DS} - V_{Dsat}$

MOSFET

- Depletion Type
  - D-type
  - P-type
- Enhancement Type
  - n-type
  - p-type

Depletion Type	Enhancement Type
1. Channel is present	1 Channel is enhance by applying by applying voltage at gate terminal.
2. Normally ON device	2. Normally off device.
3. mobility of carriers is high.	3. less in comparision to depletion type.
4. Not generally used as switch due to high threshold voltage value.	4. It is used as a switch, because of low terminal voltage.

Working principle of MOSFET:-

It act as a switch which allows & block the flow of current. when voltage is applied to the gate terminal, then an electric field is generated that changes the, width of the channel region & tends to flow the electrons.

wider channel Region ⟶ better conductivity

Structure of MOSFET

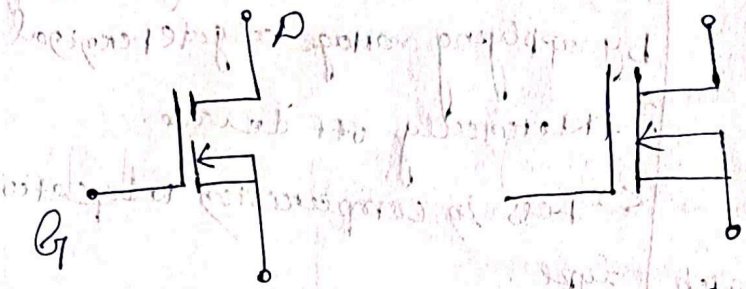
P-Type semiconductor is the base of the MOSFET. At the two side (top). of P-type two heavily doped region form. ⟶ one is source terminal & another is drain terminal (both are doped with n-type impurity)

The layer of substrate is coated with a layer of silicon dioxide for insulation.

A thin insulated metalic plate is kept on the top of the silicon dioxide & it act as a capacitor from which gate terminal is energized.

→ A DC circuit is then formed by connecting a voltage source between these two n-type regions.

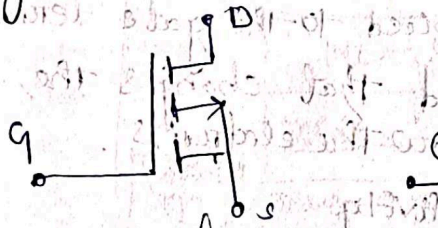
Symbol of N-channel MOSFET

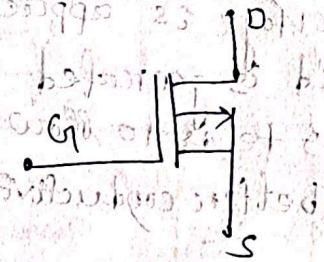


Enhancement mode

Depletion mode

Symbol of P-channel (MOSFET)





Enhancement mode

Depletion mode

Operating Regions of MOSFET :-

① Cut-off Region

In this Region there will be no conduction, MOSFET will OFF. In this Region MOSFET behaves like an open switch

② Ohmic Region / Active Region / Linear Region :-

Here, the current I_{DS} increases with increase in the value of V_{DS}. In this region, they are used as amplifiers.

③ Saturation Region

In this region, MOSFET have their I_{DS} current in spite of any increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. In this region, MOSFET act like a closed switch through which a saturated value of I_{DS} flows.

Switching Characteristics

MOSFET TYPE	$V_{GS} << 0$	$V_{GS} = 0$	$V_{GS} >> 0$
N-channel Enhancement	OFF	OFF	ON
N-channel Depletion	OFF	ON	ON
P-channel Enhancement	ON	OFF	OFF
P-Channel Depletion	ON	ON	OFF

Application of MOSFET :-

→ Radio frequency application.
→ MOSFET behaves as a passive circuit element.
→ Used to regulate DC motors.
→ Used in the design of the chopper circuit.

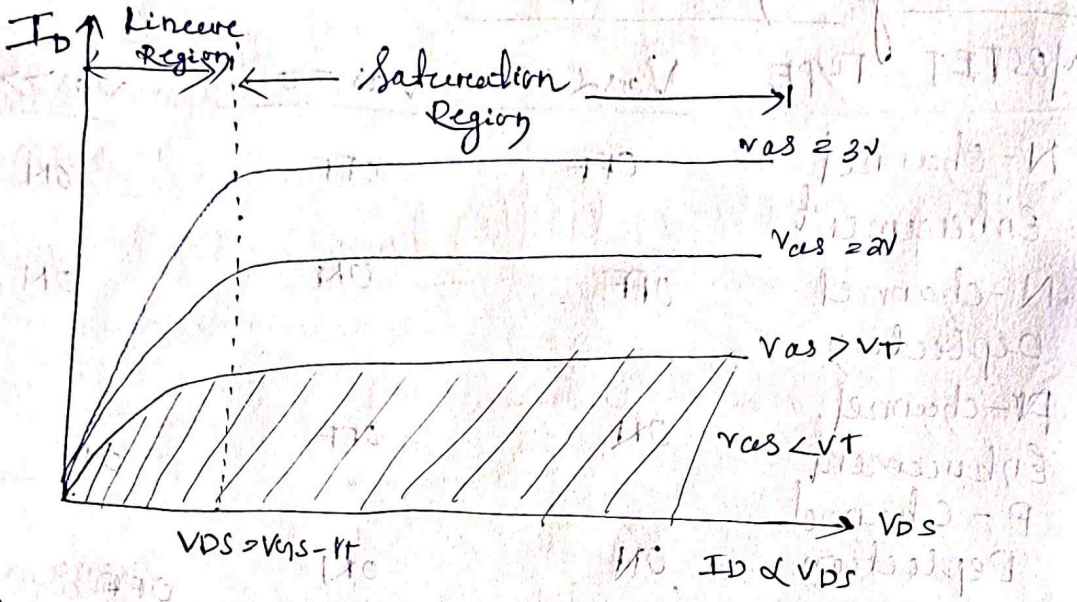
Advantage of MOSFET :-

→ operate at greater efficiency at lower voltages
→ Absence of gate current results in high input impedance producing high switching speed.

Disadvantage of MOSFET

- Damage by electronic charges due to the oxide layer.
- Overloaded voltages make MOSFET unstable.

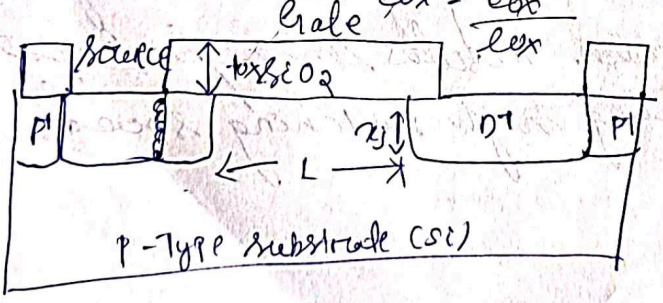
MOSFET V-I characteristics:-

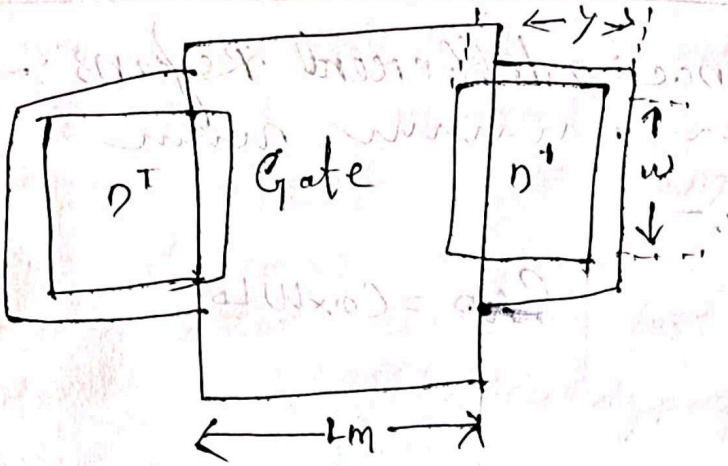


Working of MOSFET Capacitances:-

- Speed of integrated circuit is ceniured by capacitances.
- These capacitances are not lumped but distributed.
- It's values can be calculated by three mensional cross view of MOSFET.
- Here, we have already studied C_{ox} which is gate oxide capacitance, it's unit is $\mu F/cm^2$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

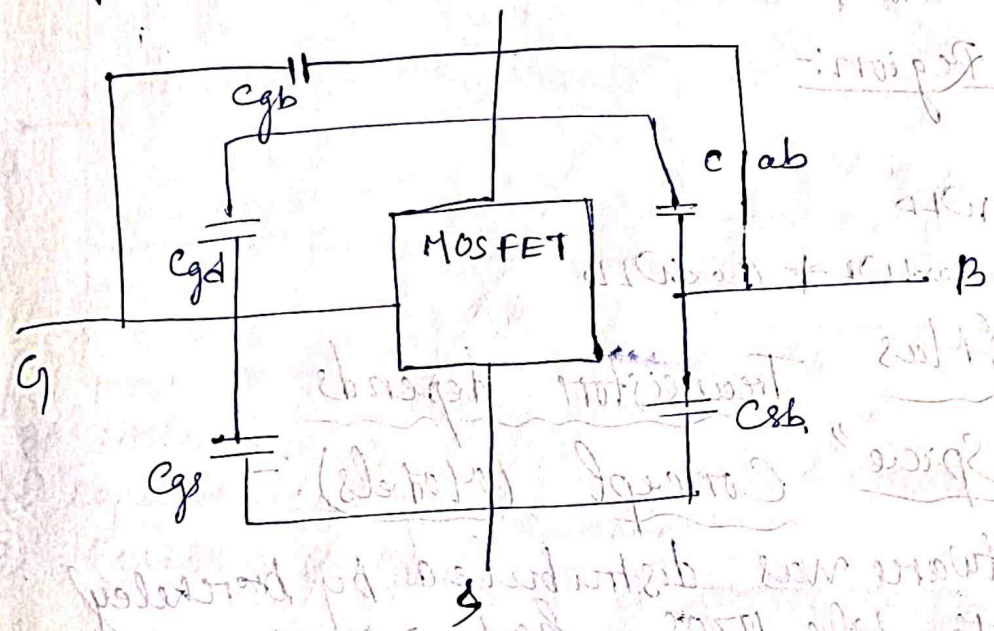




$C_{gb} = C_{ox} LW$

$C_{gs} = C_{ox} LDW$

$C_{gd} = C_{ox} L_D W$



G → Gate

D → Drain

S → Source

B → Substrate

MOSFET Capacitance in different Regions :-

Cut off Region :-

$C_{gB} = C_{ox} W L$

$C_{gs} = C_{ox} W L_D$

$C_{gD} = C_{ox} W L_D$

Linear Region :-

$C_{gB} = 0$

$C_{gD} = \frac{1}{2} \times C_{ox} W L + C_{ox} W L_D$

$C_{gs} = \frac{1}{2} C_{ox} W L + C_{ox} W L$

Saturation Region :-

$C_{gB} = 0$

$C_{gD} = C_{ox} W L_D$

$C_{gs} = \frac{2}{3} C_{ox} W L + C_{ox} W L_D$

Modeling of Mos Transistors depends "Spice" Concept (Models) :-

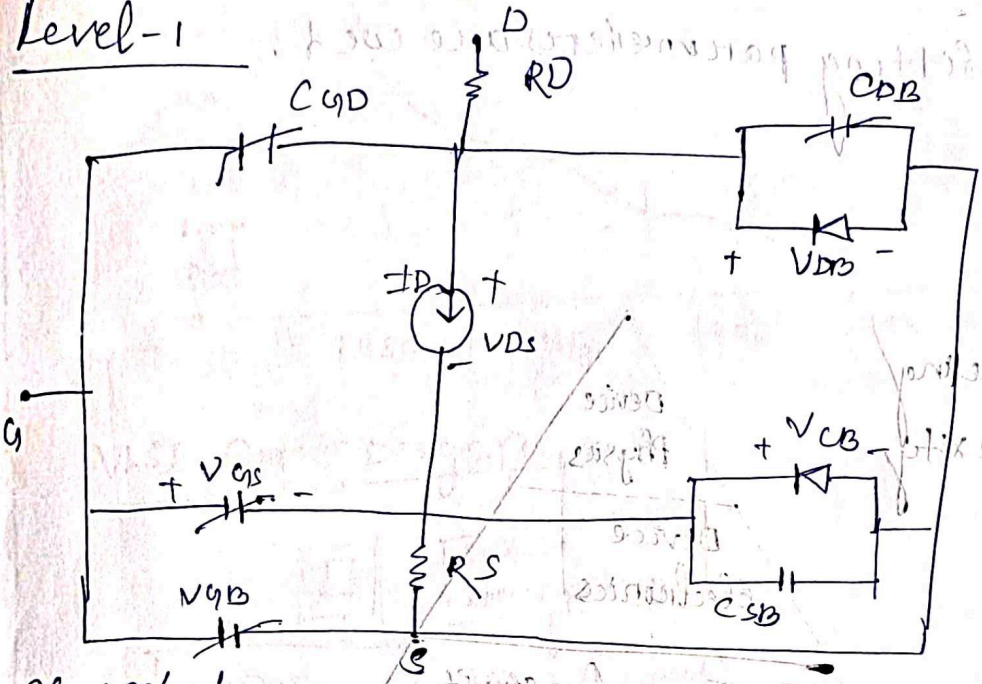
1) The SPICE software was distributed by Berkeley beginning in the late 1970s, had 3 different MOSFET Models.
2) Level 1 (MOS 1) is described by square convert voltage characteristics
3) Level 2 (MOS 2) is detailed analytical MOSFET Model.
4) Level 3 (MOS 3) is a semi-empirical model
Both MOS 2 & MOS 3 includes second-order effect.
SPICE Model is used to predict the behaviour of some part under varying.

Conditions by the help of SPICE simulations, where we use text description of a circuit component

SPICE → Simulation program with integrated circuit emphasis

It is a tool used to test designs prior to potentially costly prototyping

Level-1



It includes (1) Resistance of source & Drain
(2) Capacitance (bias dependent)
(3) Reverse - Bias behaviour of Junction Diode

Level-2 :-

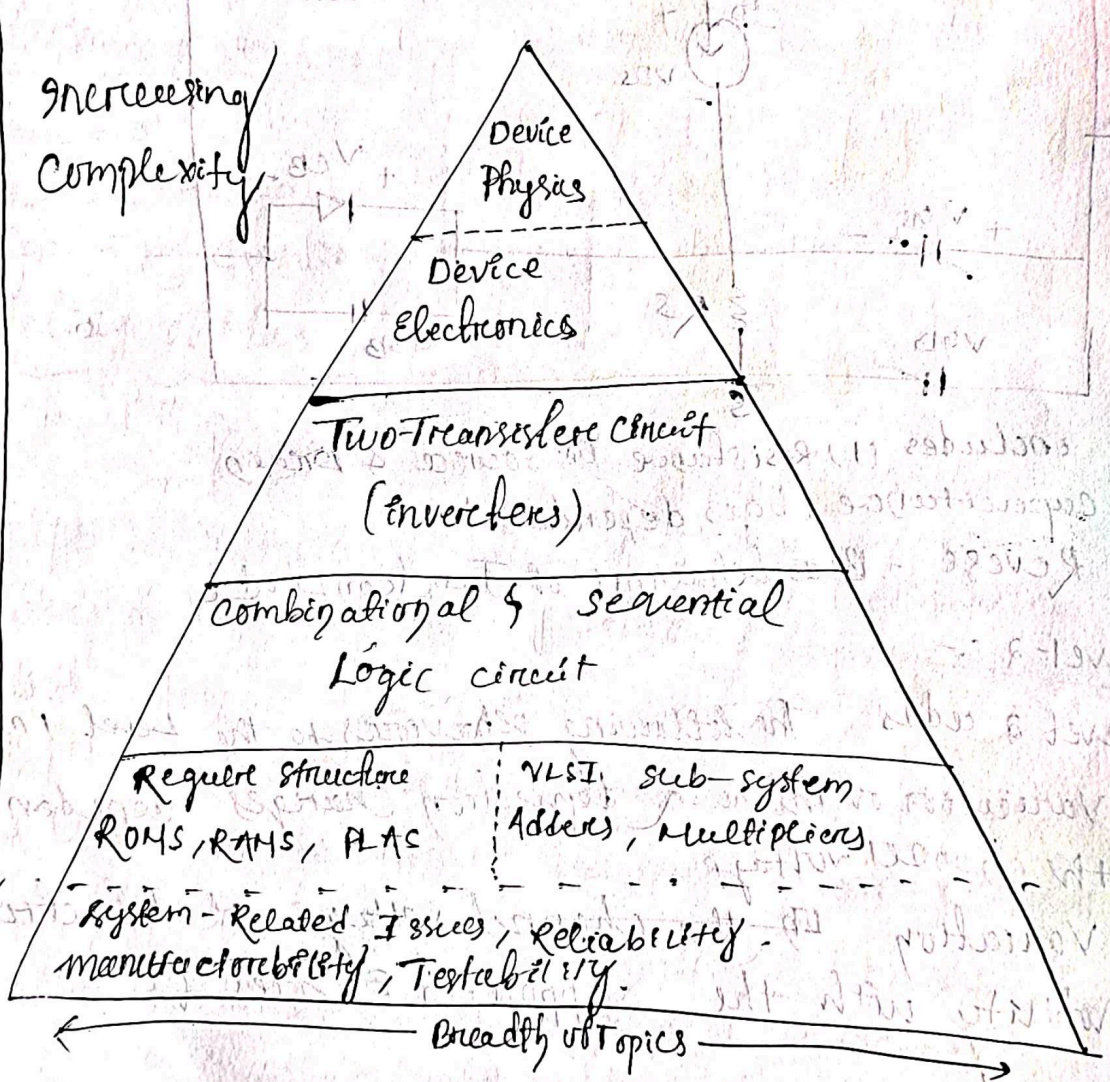
Level 2 adds the following behaviours to the Level 1 model :-
(1) Variation of the bulk depletion charges dependance on the channel voltage.
(2) Variation ~~in the channel voltage~~ of Electrons Mobility with the applied E-field.

(3) Variation of effective channel length & saturation mode
(4) Carrier velocity saturation.
(5) Sub threshold conduction.

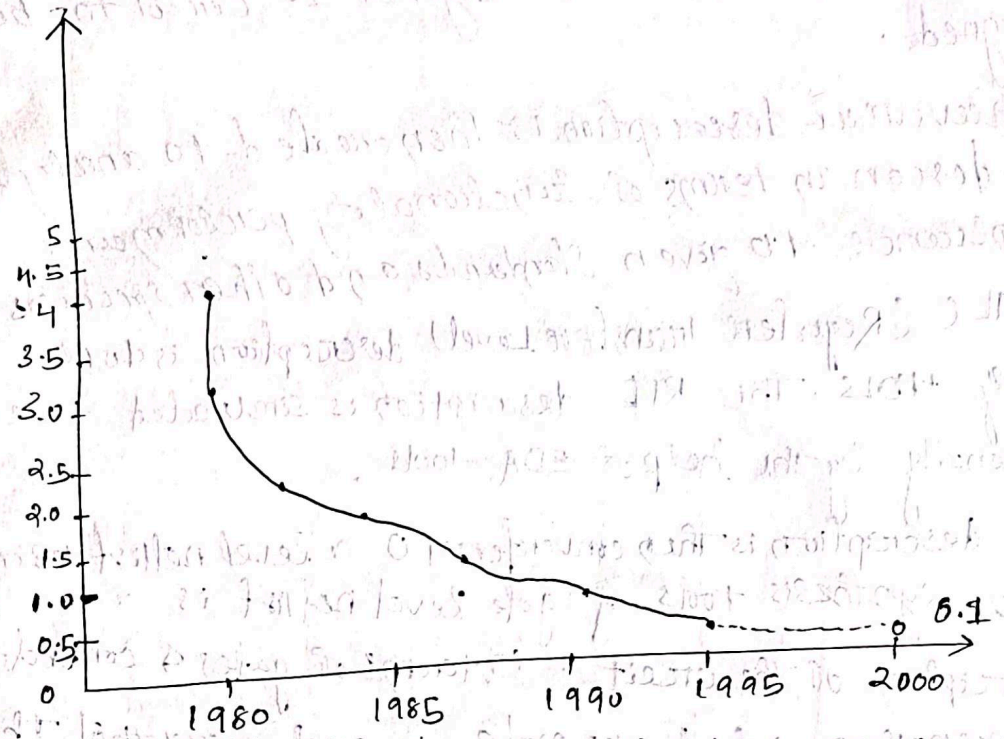
Level 3 :-

→ Level 3 was developed to specifically address small geometry effects.

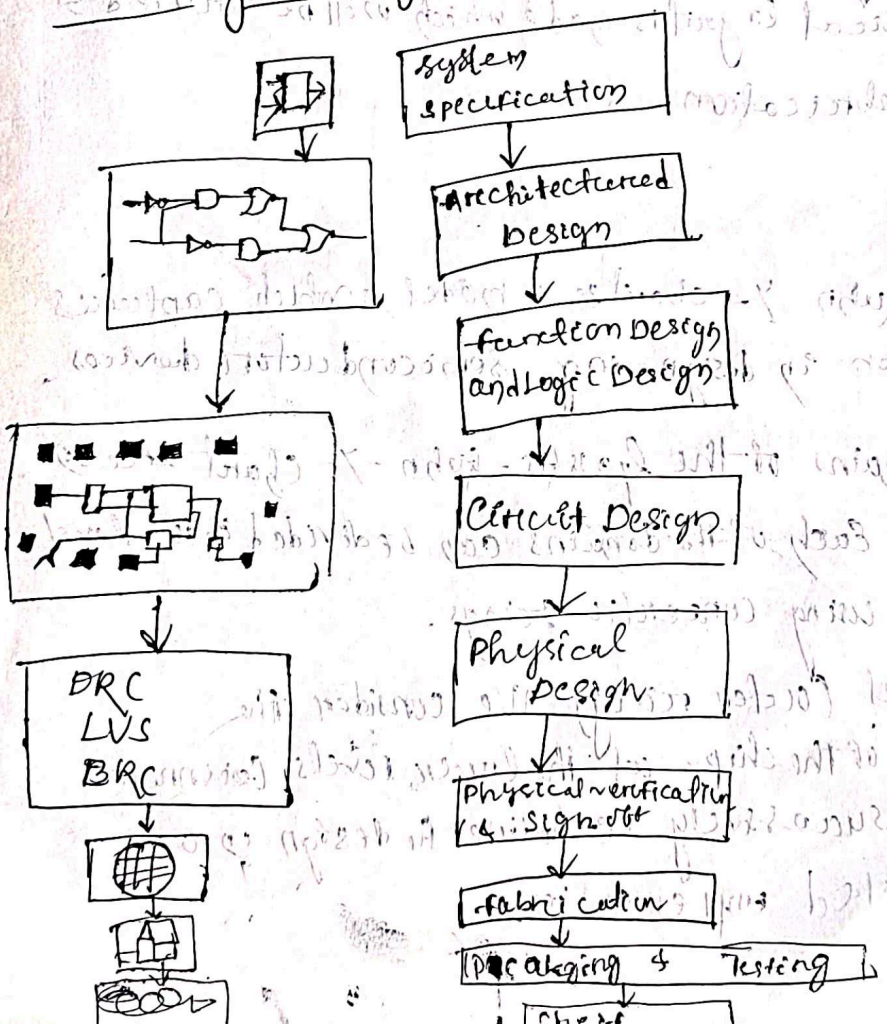
→ Curve fitting parameters are used.



Evolution of minimum feature size in IC over time :-



VLSI ~~Design~~ Design flow:-



→ First comes specifications, then functionality, interface & the architecture of the digital IC circuit to be designed.

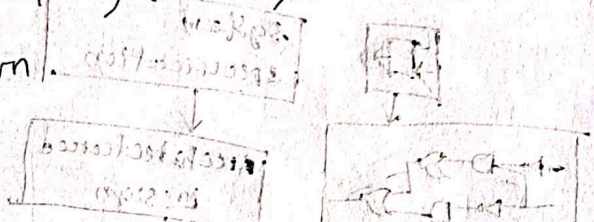
→ Behavioral description is then created to analyze the design in terms of functionality performance, compliance to given standards and other specifications.

→ RTL (Register transfer Level) description is done using HDLs. This RTL description is simulated to test functionally by the help of EDA tools.

→ RTL description is then converted to a level netlist using logic synthesis tools. A gate level netlist is a description of the circuit in terms of gates & connections between them, which are made in such a way that they meet the timing, power & area specifications.

→ Finally, a physical layout is made which will be verified & then sent to fabrication.

Y-chart :-



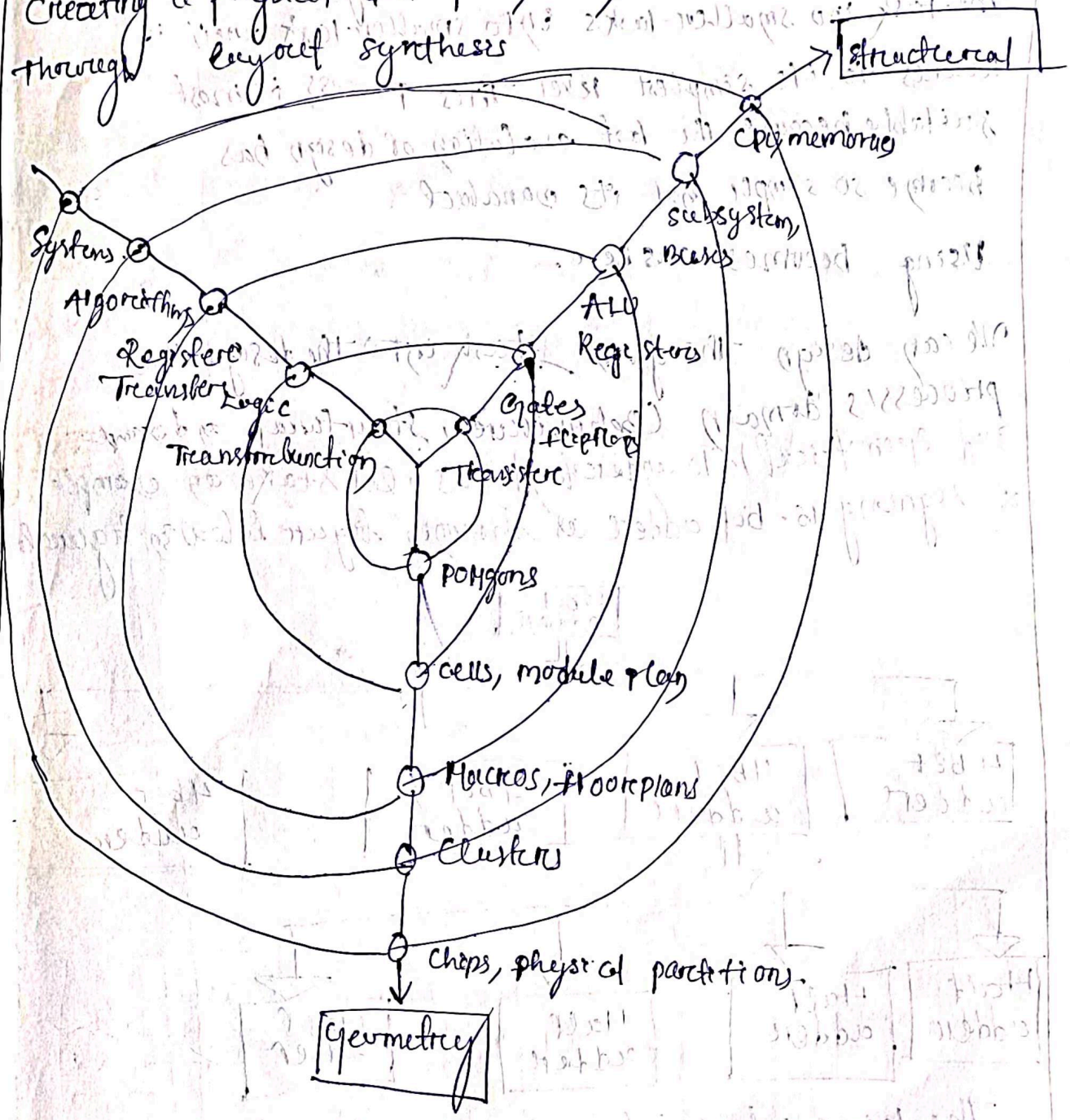
→ The Gajski-Kuhn Y-chart is a model, which captures the consideration in designing semiconductor devices.

→ The three domains of the Gajski-Kuhn Y-chart are on radial axes. Each of the domains can be divided into level of abstraction using concentric rings.

→ At the top level (outer ring) we consider the architecture of the chip, at the lower levels (inner rings), we successively refine the design into it for detailed implementation.

→ Creating a structural description from a behavioral one is achieved through the process of high-level synthesis or logical synthesis.

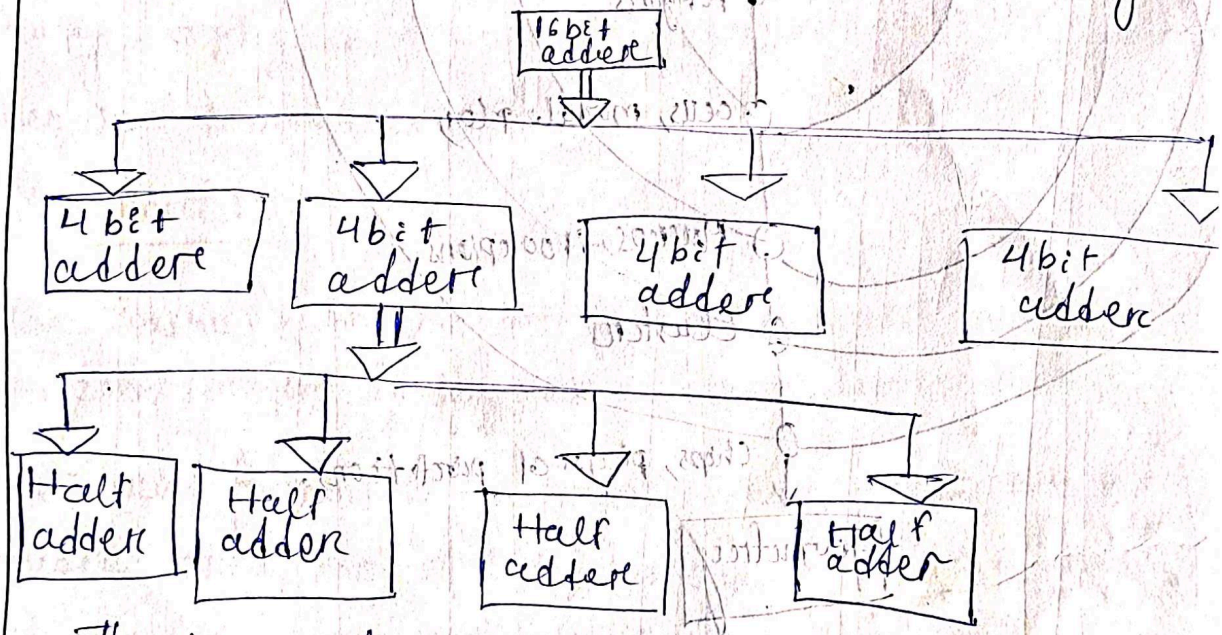
→ Creating a physical description from a structural one is achieved through layout synthesis



Design Hierarchy - structural :-

The design hierarchy involves the principle of "Divide and conquer". This is nothing but dividing the task into smaller tasks into smaller task until it reaches to its simplest level. This process is most suitable because the last evolution of design has become so simple that its manufacture & using becomes easier.

We can design the given task into the design flow process's domain (Behavioural, structural and geometrical). To understand this, let's take an example of designing 16-bit adder as shown in figure below in figure.



The hierarchical design approach reduces the design complexity by dividing the large system into several sub-modules.

The hierarchical design approach meets satisfy the concept of Regularity, modularity, locality.

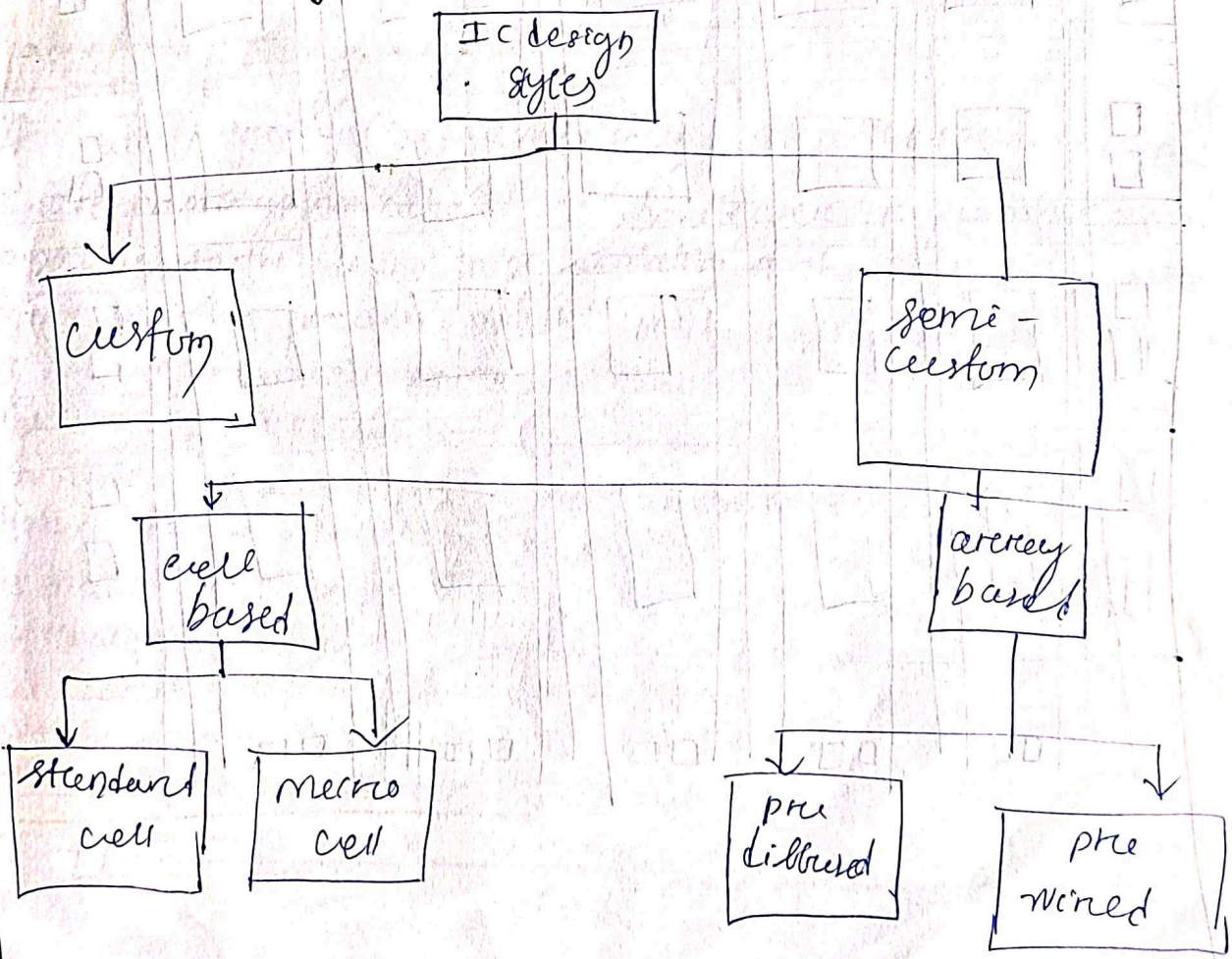
Regularity → It means the hierarchical decomposition of large system should result in not only simple, but also ~~similar~~ identical blocks, as much as possible.

EX: design of array structures consisting of identical cells such as a parallel multiplication array.

Modularity — The various functional block which make up the larger system must have well defined functions & interfaces

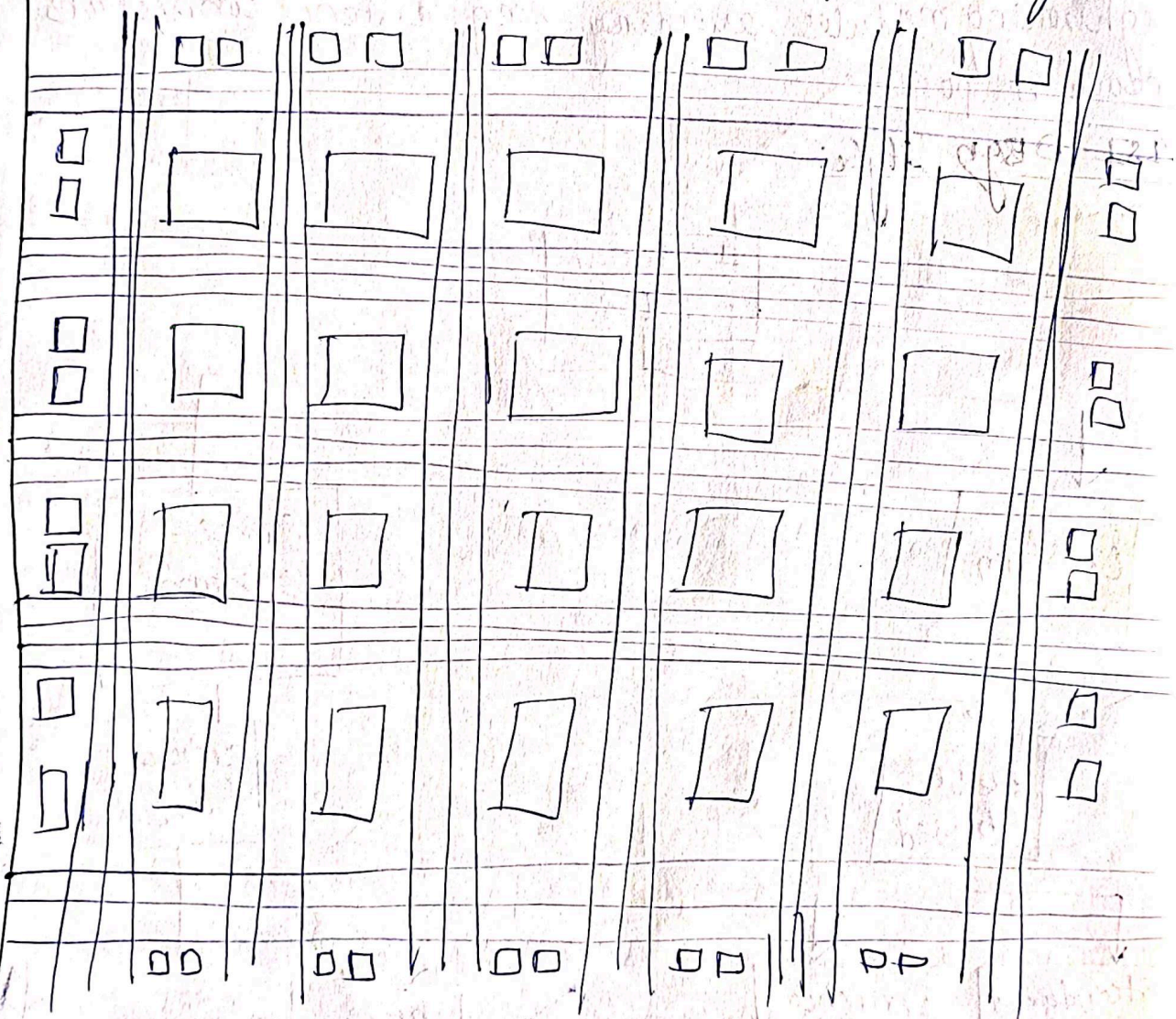
Locality → It ensures that connections are mostly between neighboring modules, avoiding long distance connections as much as possible.

VLSI Design style:-



FPGA:- "Field programmable Gate Array" :-

It contains ten thousand to more than a million logic gates with programmable interconnection. programmable interconnection are available here users or designers to perform given functions easily. From the figure, there are I/O blocks, which are designed & numbered according to function for each module. At logic level composition, there are CLBs (Configurable Logic Block



CLB performs the logic operation given to the module. The interconnection between CLB and I/O blocks are made with the help of horizontal routing channels, vertical routing channels & PSM (programmable multiplexers).

The no. of CLB it contains only decides the complexity of FPGA. The functionality of CLB's and PSM are designed by VHDL or any others hardware descriptive language after programming CLB & PSM and placed on chip and connected with each other with routing channel.

Advantages:- It requires very small time; Starting from design process to functional chip.

① No physical manufacturing steps are involved in it.

② The only disadvantage is it is costly than other styles.

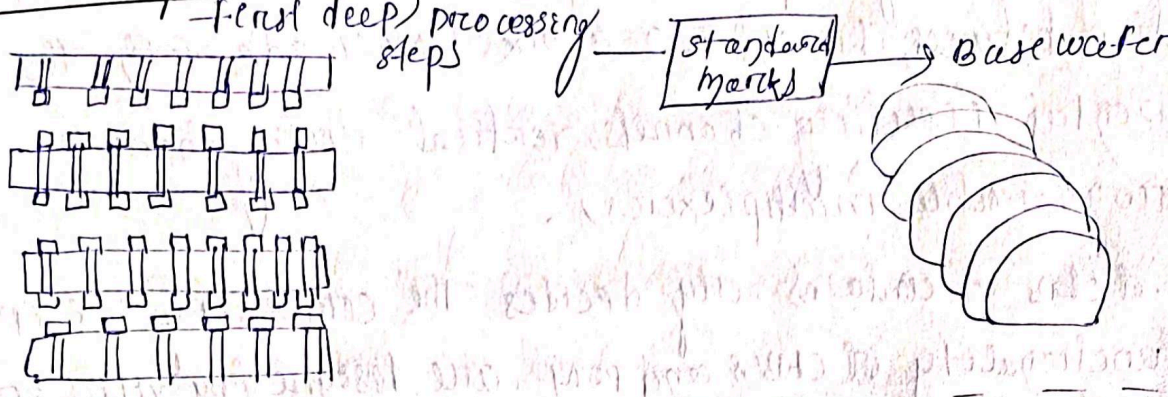
Gate Array Design:-

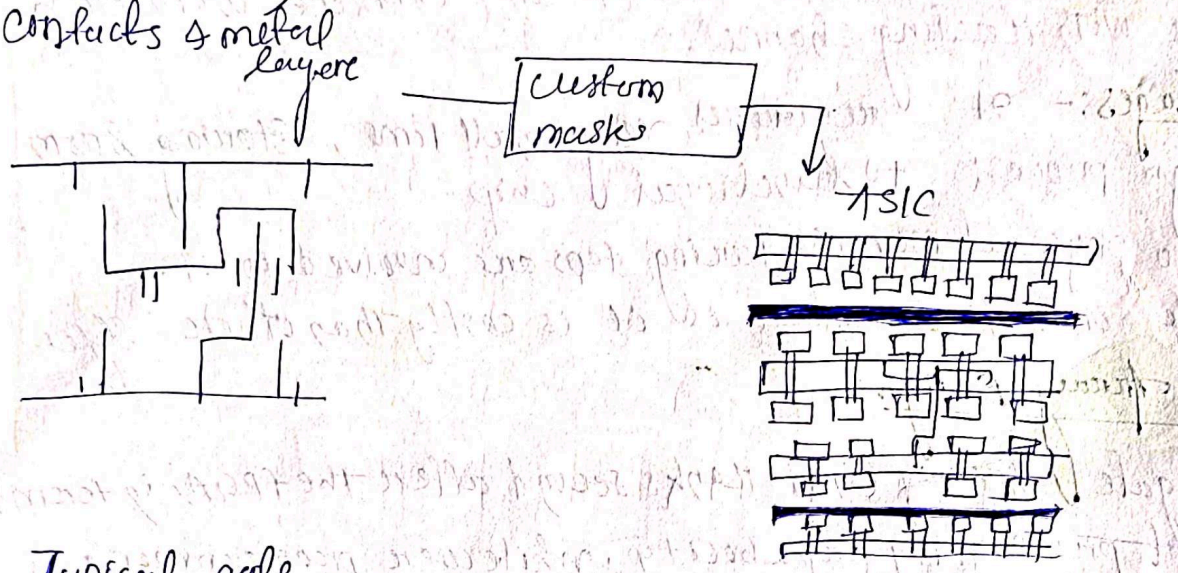
The gate array (GA) ranks second after the FPGA, in terms of fast prototyping capability. While user programming is important to the design implementation of the FPGA chip, metal mask design & processing is used to GA. GA implementation requires a two-step manufacturing process.

The first phase results in an array of uncommitted transistors on each GA chip. These uncommitted chips can be stored for later customization, which is completed by defining the metal interconnects between the transistors of the array. The patterning of metallic interconnects is done at the end of the chip fabrication process, so that the turnaround time can still be short, a few days to a few weeks.

Two-step manufacture:-

Two-step manufacture





Typical gate array platforms use dedicated areas called channel, for inter-cells routing between rows or columns of MOS transistors. They simplify the interconnections. Interconnection patterns that perform basic logic gates are stored in a library, which can then be used to customize rows of uncommitted transistors according to netlist.

In most of the modern GAs multiple metal layers are used for channel routing. With the use of multiple interconnected layers, the routability can be achieved over the active cell areas, so that the routing channels can be removed as in sea-of-gate GAs/ chips. Here the entire

Chip surface is covered with committed nMOS PMOS transistors. The neighbouring transistors can be customized using a metal mask to bond basic logic gates.

For inter cell routing, some of the uncommitted transistors must be sacrificed. This design style results in more flexibility bcoz inter connections and usually in a higher density. Of chip utilization factor is measured by the used chip area divided by the total chip area, it is higher than that of the FPGA & so is the chip speed.

Standard cell Based Design:-

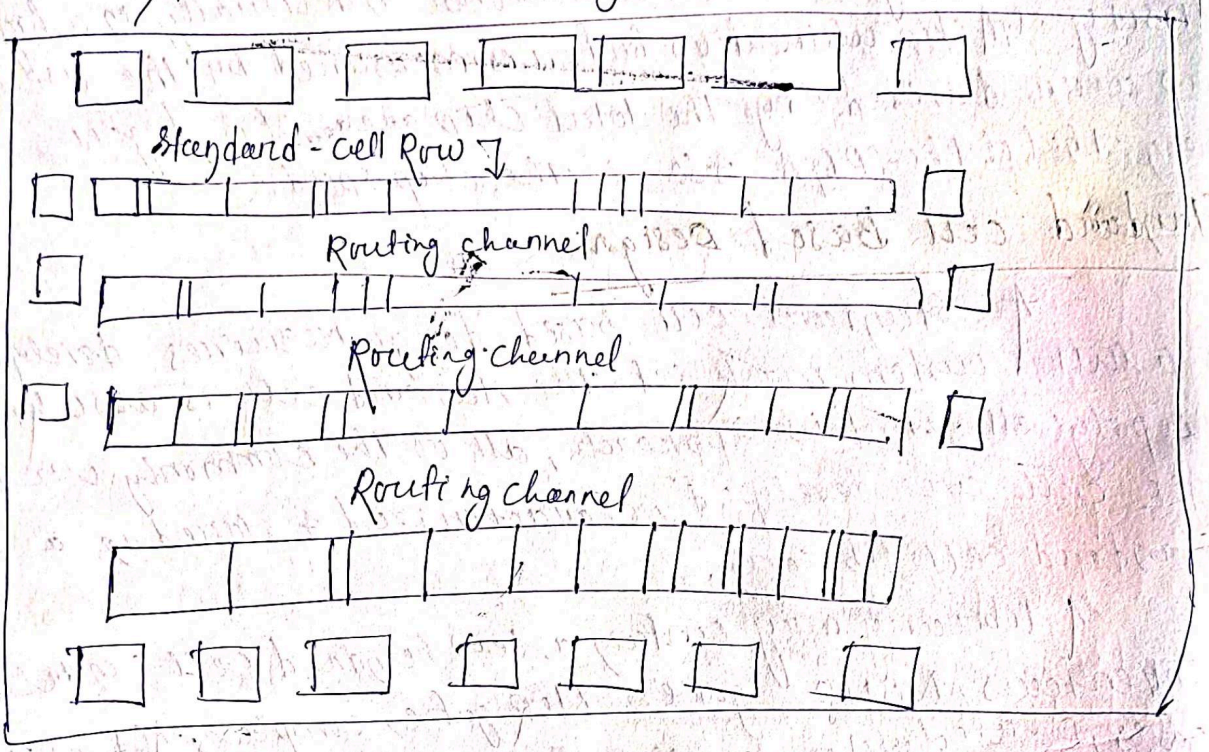
↑ Standard cell based design requires development of a full custom mask set. The standard cell is also known as the poly cell design. In this approach, all of the commonly used logic cells are developed, characterized & stored in a standard cell library.

↑ library may contain a few hundred cells including inverters, NAND gate, XOR gate, complex, AOI, OAI gates, D-flip flops & flip-flops. Each gate type can be implemented in several versions to provide adequate driving Capability: bcoz different bcoz loads. The inverter gate can have standard size, double size, and quadruple size so that the chip designer can select the proper size to obtain high circuit speed & layout density.

Each cell is characterized according to several diff. characterization categories such as:-

- Delay time versus load capacitance
- Circuit simulation model.
- Timing " "
- Fault " "
- Cell data for place and route.
- Mask data.

- For customized placement of the cells & routing, each cell layout is designed with a fixed height, so that a no. of cells can be bounded side by side to form rows. The power & ground rails run parallel to the upper & lower boundaries of the cell. So that, neighboring cells share a common power bus & a common ground bus.



Full custom Design:-

In a full-custom design, the entire mask design is made new, without the use of any library. The development cost of this design style is rising. Thus, the concept of design reuse is becoming famous to reduce design cycle times & development cost.

The hardest full custom design can be the design of memory cell, be it static or dynamic. For logic chip design, a good negotiation can be obtained using a combination.

of different design styles on the same chip i.e standard cell+ data / path cells, & programmable logic arrays (PLAs).

practically the designer does the full custom layout i.e the geometry, orientation and placement of every transistor. The design productivity is usually very low; typically a few tens of transistors per day, per designer. In digital CMOS VLSI, full custom design is hardly used due to the high labour cost. These design styles include the design of high volume products such as memory chips high performance microprocessors & FPGA

CHAPTER - 2

FABRICATION OF MOSFET

Simplified process sequence for fabrication :-

→ CMOS fabrication technology requires both NMOS and PMOS transistors to built on the same chip substrate.

→ To accomodate both NMOS & PMOS devices special regions must be created in which the semiconductor type is opposite to the substrate's type, These special regions are called wells or tubs

→ so, an n well is formed in a p substrate & a ~~simplified~~ p well is formed in a substrate.

Simplified process sequence :-

→ The process starts with the creation of the n well regions for PMOS and p well regions for NMOS by ion implantation into the substrates.

→ Ion implantation is the process of adding impurities to a silicon wafer.

→ Then a thick oxide is grown in the regions surrounding the NMOS & PMOS active regions, the thin gate oxide is subsequently grown on the surface through thermal oxidation.

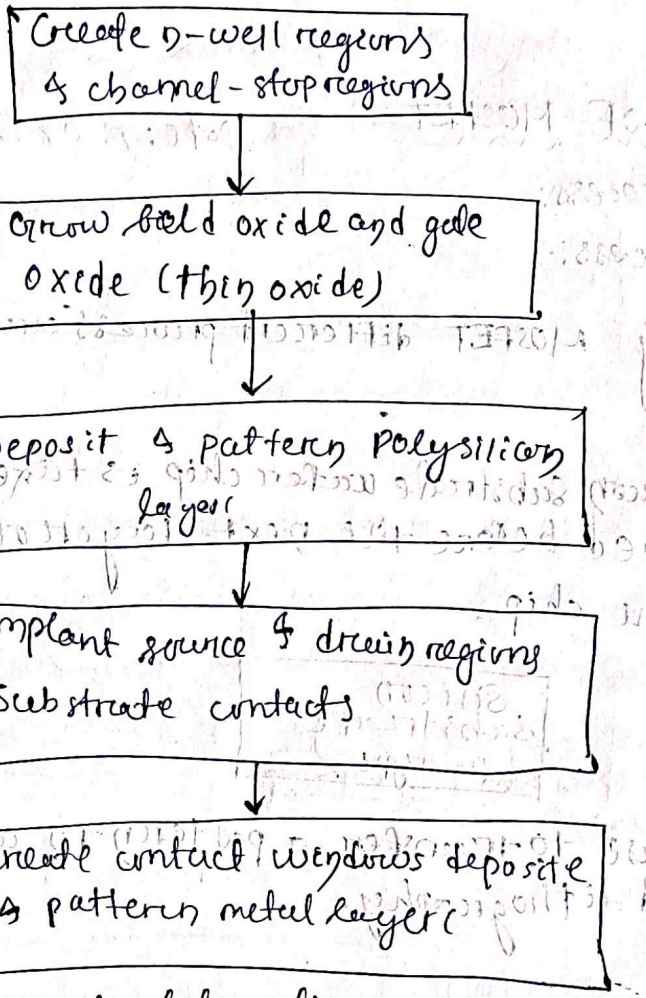
→ Again a polysilicon layer is deposited on the surface of the oxide layers & selectively removed to form the gates.

→ These steps are followed by the creation of n^+ and p^+ regions.

→ At last ~~metal~~ metalization is done means creation of metal interconnects.

→ metalization is the process by which the components of IC's are interconnected by aluminium conductors.

→ Channel stop implant is used to prevent the formation of any unwanted channels between two neighboring regions, Hence channel stop implants act to electrically isolate neighboring devices built on the same substance.



Basic steps of fabrication

→ The fabrication cycle of VLSI chips consists of a sequential set of basic steps which are wafer preparation, oxidation, lithography & etching.

→ During fabrication process, the devices are created on the chip. So IC may be viewed.

→ During fabrication process, the devices created on the chip, so, IC may be viewed.

as a set of patterened layers.

→ A layer must be patterened before the next layer of material is applied on the chip.

→ patterning uses the process of lithography. The process used to transfer a pattern to a layer on the chip is called lithography.

→ The lithography sequence must be repeated for every layer.

3. Febricedion OF MOSFET Date: 7:08:2012

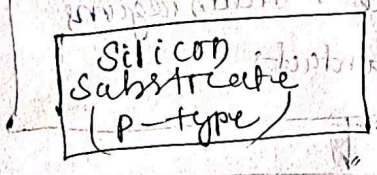
Febricedion process:-

Fabrication process:-

For fabricating MOSFET different process are used.

Step-1

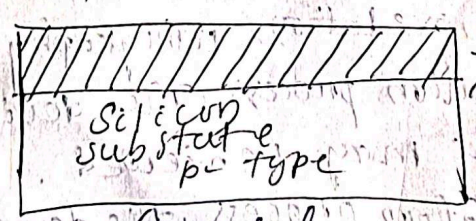
→ At first a silicon substrate wafer chip is taken. The layers must be patterned before the next layer of material is applied on the chip.



→ The process use to transfer a pattern to a layer on the chip is called lithography.

Step-2

→ The silicon surface is oxide by using oxidation process to form an oxide layer on the silicon surface.

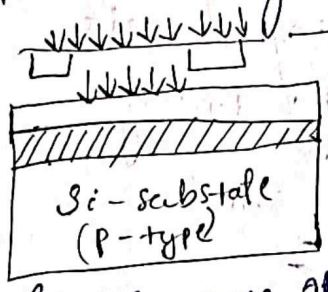


→ sio2 (Insulating layer)

Si + O2 → SiO2 (Insulating layer)

Step - 3

on the surface SiO_2 photoresist layer is added which is sensitive to the light.



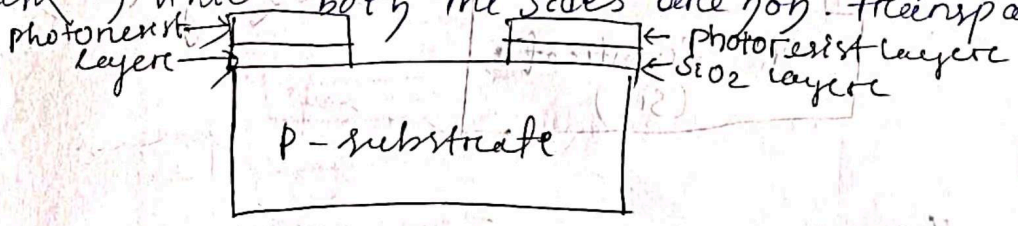
→ The photoresist layers are of 2 layers
(1) positive photoresist layer
(2) Negative photoresist layer.

→ when photoresist layer come in contact with ultraviolet light & it is soluble, then it is called as positive photoresist layer.

→ when photoresist layer come in contact with ultraviolet light & it is insoluble then it is called as negative photoresist layer.

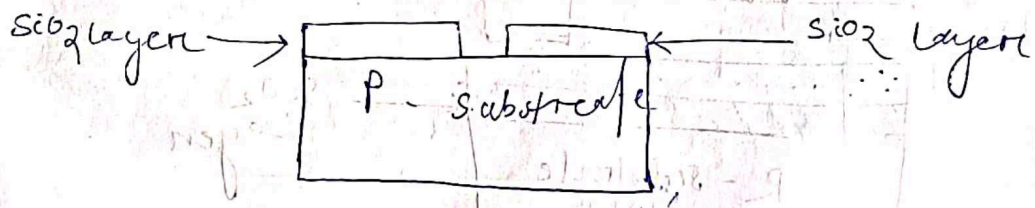
→ Usually positive photoresist layer is used

→ to remove the photoresist layer & silicon dioxide layer (SiO_2) the ultraviolet light is pass through a transparent mask in which both the sides are non-transparent.



Step-4

After the step no. 3 photoresist layer is present on both the side. The photoresist layer can be be remove by a solvent (Hydrofluoric acid) or plasma etch.



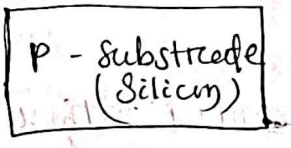
→ The process of removing the remaining photoresist from SiO_2 surface using solvent (is leaving the pattern on the SiO_2 surface is called as etching process.

→ For accurate generation of high density.

Fabrication of n-MOS :-

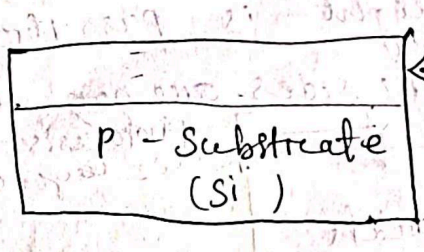
Step-1

A thick silicon wafer substrate is taken which is p-type and the surface of silicon is pattern.



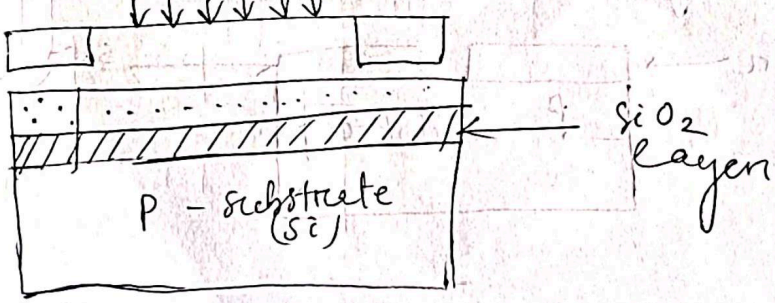
Step-2

Add SiO_2 on the surface of p-substrate or silicon substrate by the help of oxidation process. The surface of SiO_2 is patterned.

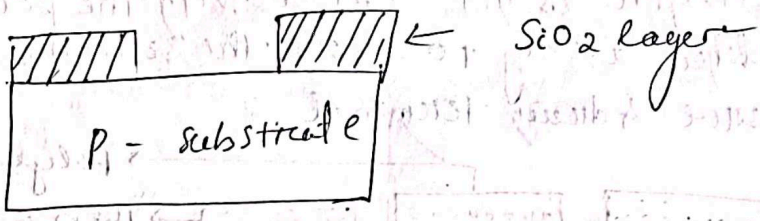


Step-3

Remove the SiO_2 by the help of the photoresist layer. then the ultraviolet light is passed through the help of mask which is non-transparent at both the sides transparent at the middle.

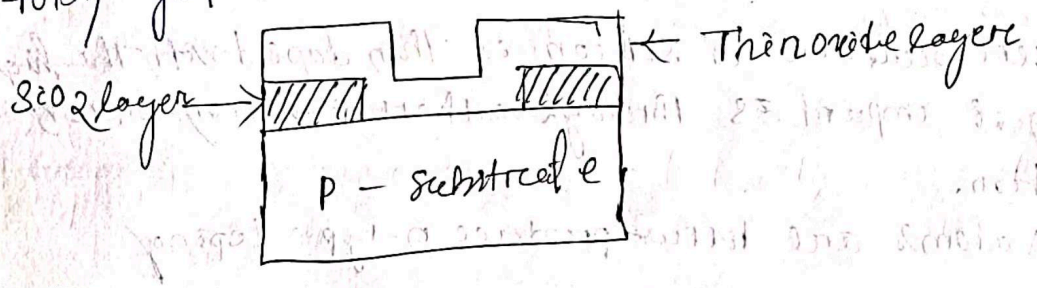


→ The remaining photoresist layers is removed by the help of etching process.



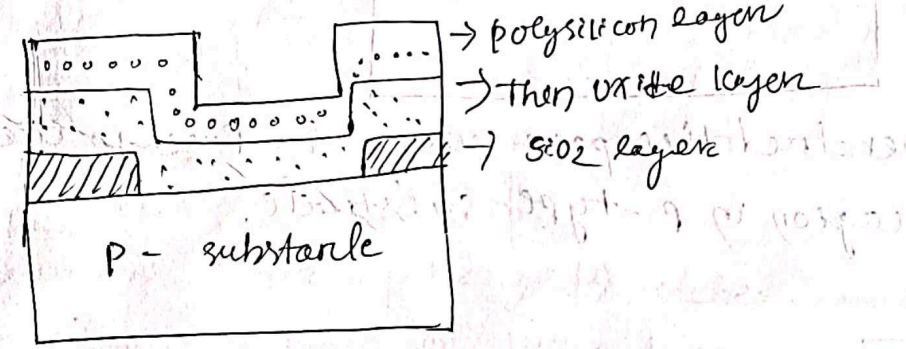
Step-4

After that a thin oxide layer is passed on entire surface of silicon - substrate which is a high density oxide layer to form gate oxide of MOSFET.



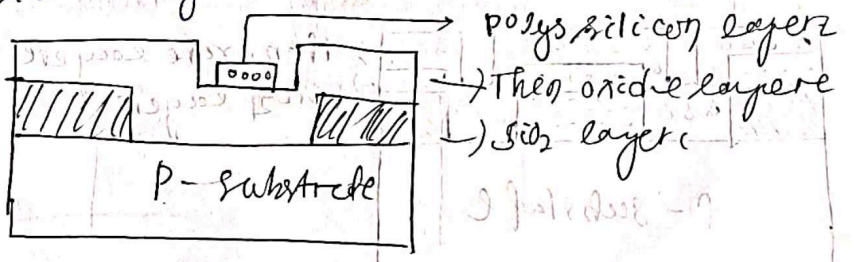
Step-5

On the top of thin oxide a poly silicon layer is added. The polysilicon layer is used both as a gate terminal & interconnect medium in silicon IC.



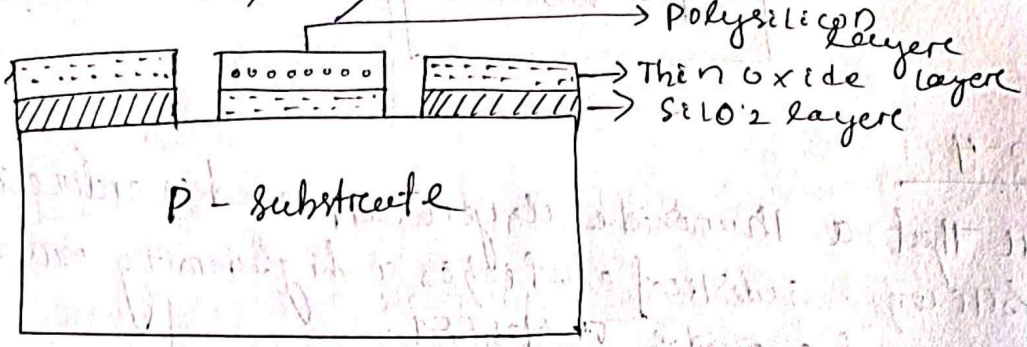
Step-6

The polysilicon layer is patterned & etched to form interconnects & MOS - transistor gate.



Step-7

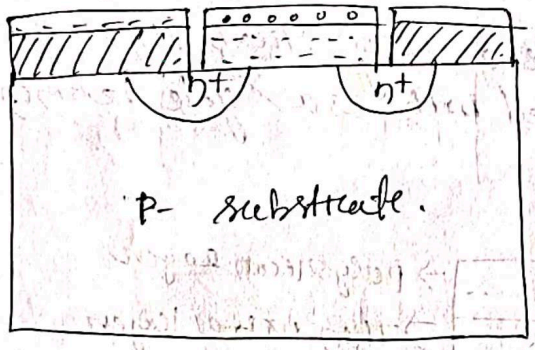
Thin oxide layer is got covered with the poly silicon layer is also etched away to expose the silicon substrate to form source & drain terminal.



Step-8

The entire surface of silicon is then doped with the high concentration of impurities through either diffusion or ion implementation.

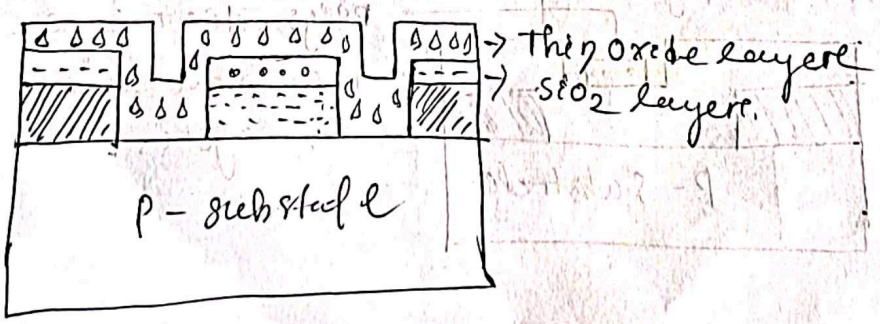
→ The Dopant atoms are diffuse produce n-type doping



→ Doping penetrated the expose silicon surface to create the n-type region in p-type substrate.

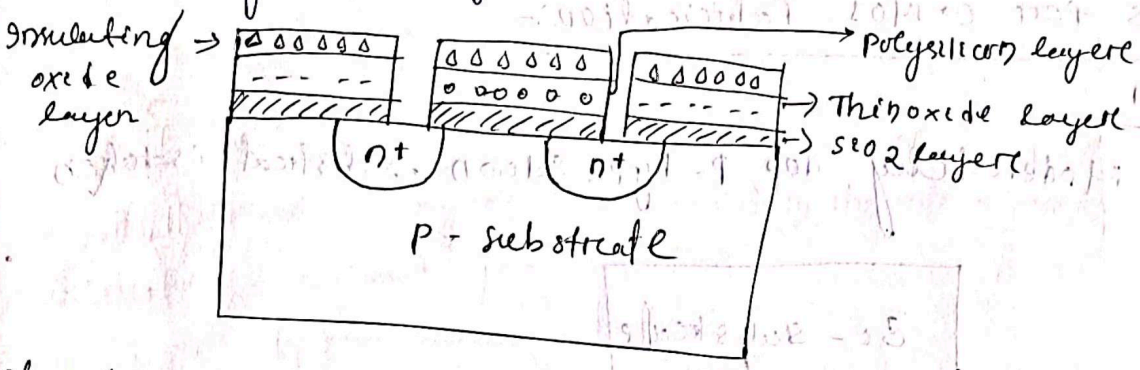
Step-9

At the top of the silicon surface insulating layers is used (SiO_2)



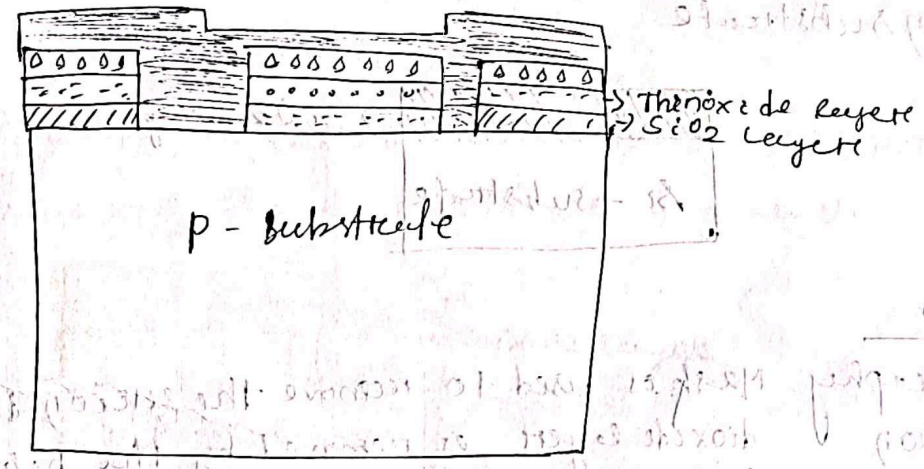
Step - 10

The insulating layer is patterned to provide a contact windows for drain & source junction. Etching process is used to remove the insulating oxide layers.



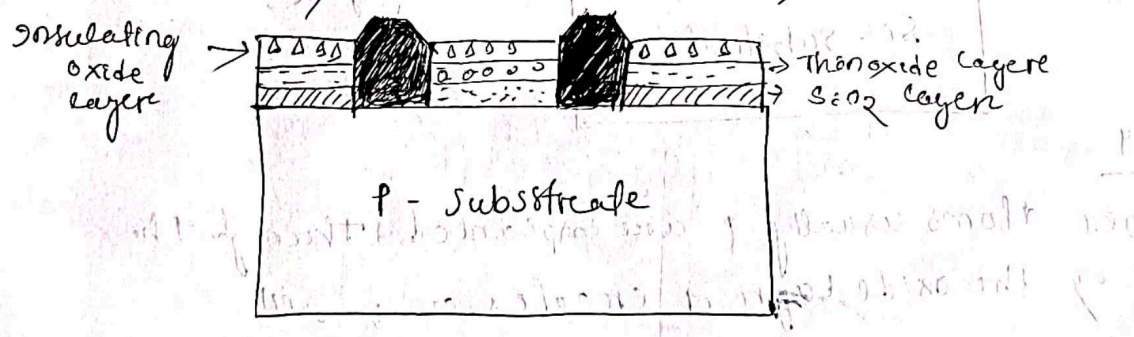
Step - 11

Again the surface is covered with the evaporated aluminium which will form the inter connection



Step - 12

Finally the metal layers is patterned & etched, completing the inter connection of MOS on silicon surface



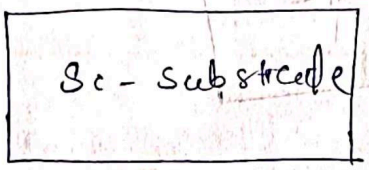
Fabrication of C-MOS
(C-MOS - complementary MOSFET) :

→ We known that MOSFETs are of two types P-MOS & N-MOS
→ The C-MOS is used which consists of both P-MOS & N-MOS

Steps for C-MOS fabrication :-

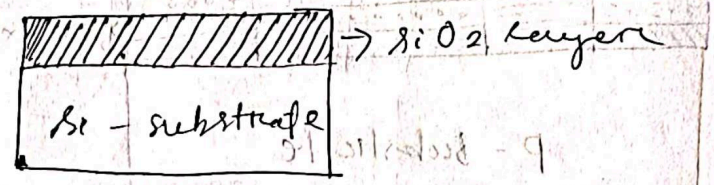
Step-1

First Moderately dop P-type silicon substrate is taken



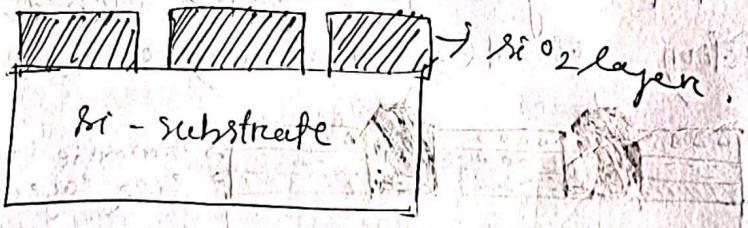
Step-2

A silicon dioxide layer is drawn on entire surface of silicon substrate



Step-3

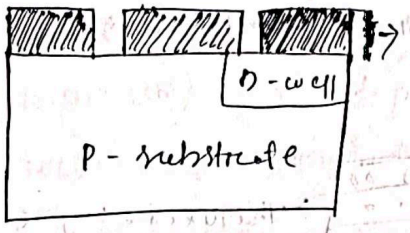
Lithography process & Mask is used to remove the silicon dioxide layer. The silicon dioxide layer is removed by the help of etching photoresist layer is used to remove the SiO_2 layer.



Step-4

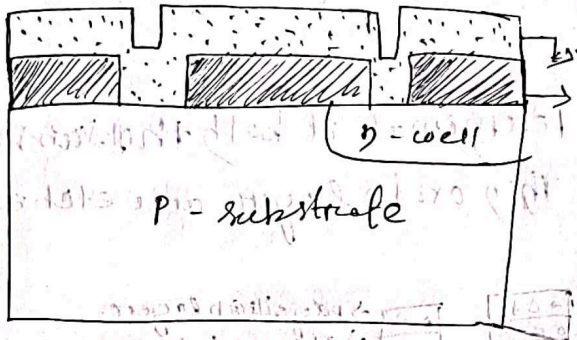
→ The donor atoms usually P are implanted through the window of the oxide layer it creates a n-well

After that active areas of n-mos & p-mos transistors can be defined.

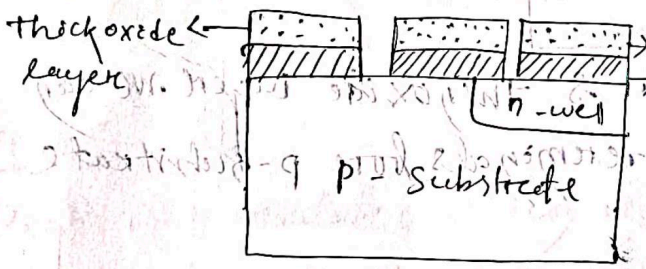


Step -5

The Thick oxide layers is applied on the entire surface of p-substrate & n-well

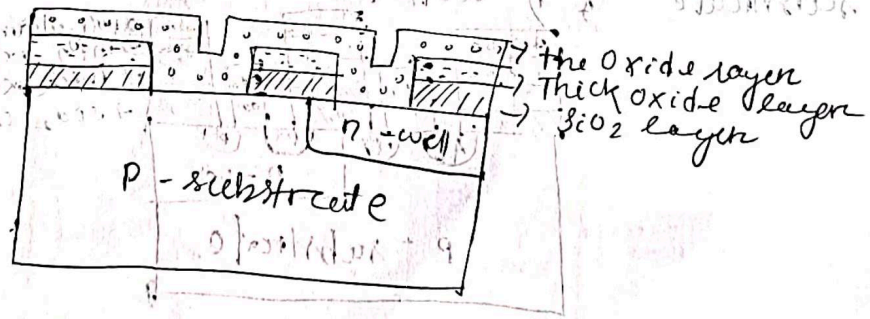


→ Then it goes for etching process which removes the thick oxide layers from both the p-substrate & n-well



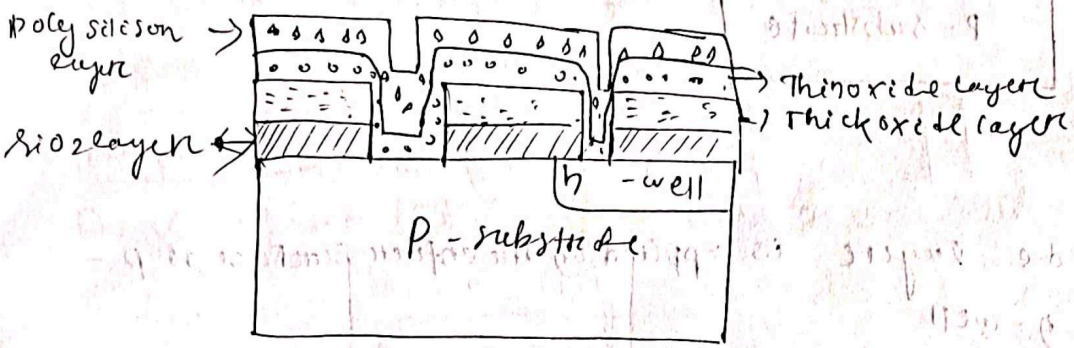
Step -6

The Thin oxide layers is passed on entire surface of p-substrate & n-well



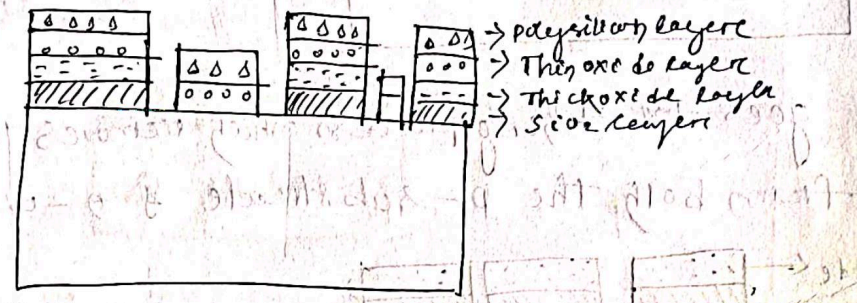
Step-7

A polysilicon layer is added on the entire surface of p-substrate & n-well



Step-8

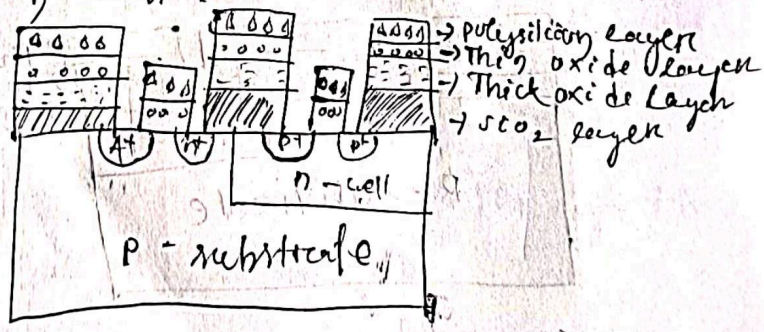
For drain & source terminal at both the p-substrate & n-well polysilicon layer & thin oxide layer are etched or remove.



→ By etching polysilicon layer & thin oxide layer we can able to get the gate terminals both p-substrate & n-well.

Step-9

By using a set of two mask n^+ & p^+ regions are implanted into the p-substrate & n-well.

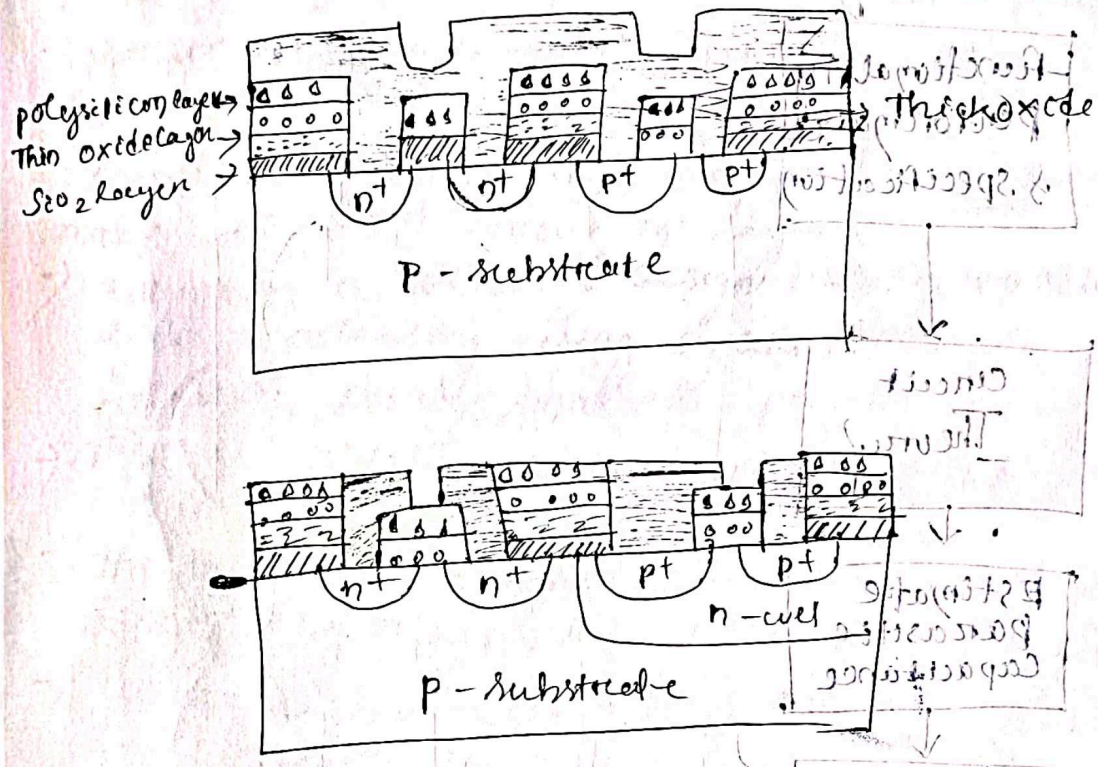


Step-10

→ Ohmic contact to the substrate & n-well are implanted.

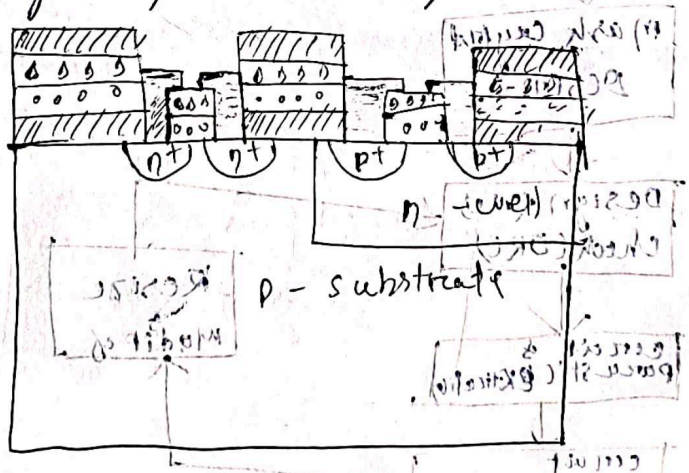
→ The metals (Aluminicon) are deposited on the entire surface of substrate & n-well using metal evaporated.

→ Then metal lines are patterned through the etching process



Step-11

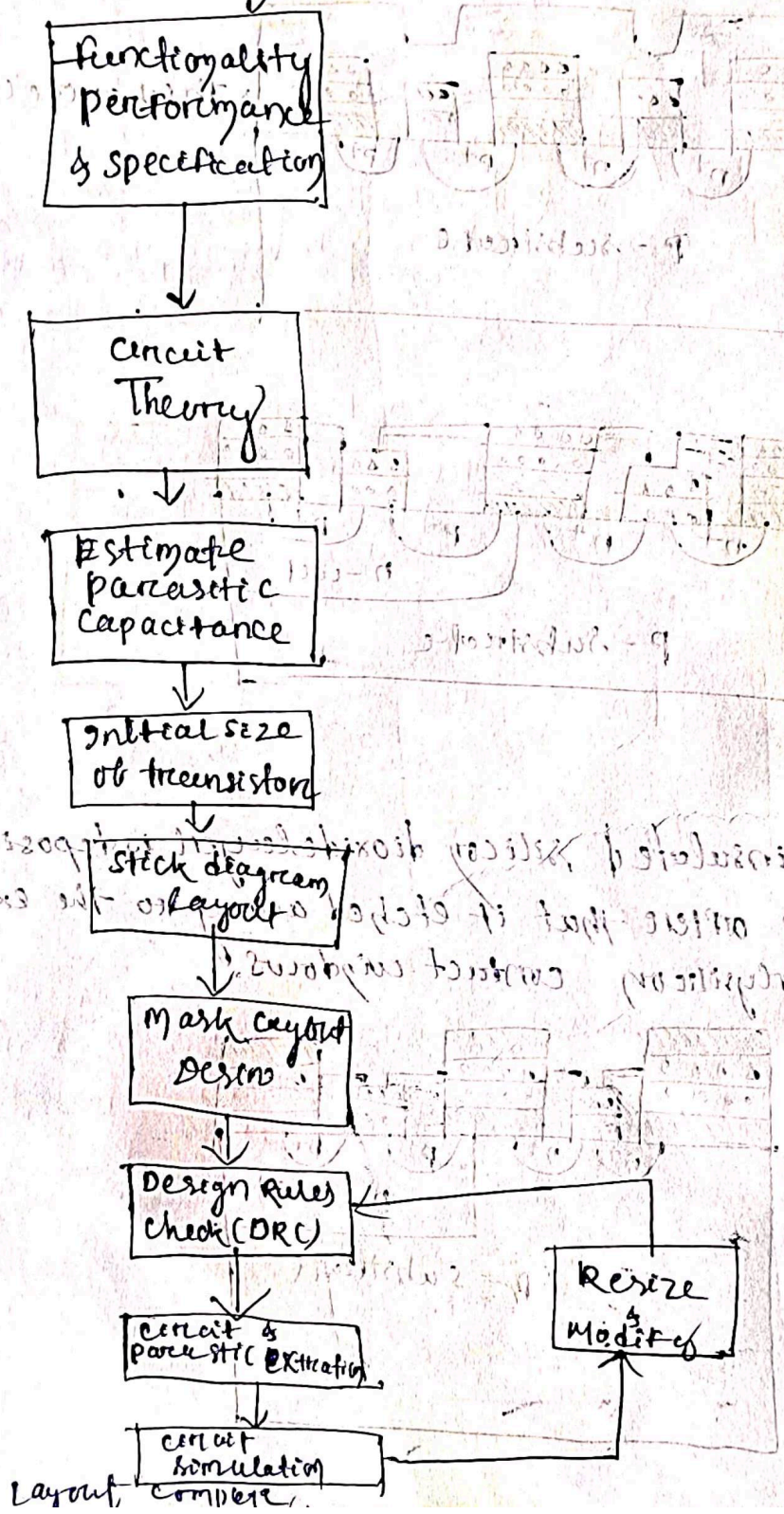
→ Finally an insulated silicon dioxide layer is deposited on the entire wafer after that it etched away to the expose silicon or polysilicon contact windows.



Linear, proportional scaling of all Geometrical constraints.
constraints

→ Lambda based layout design Rules simplified the industry standard micro based design Rules. It allows scaling property for various process.

Full custom Mask layout design



Layout design Rules

→ Layout of any circuit to manufacture using a particular process most conform to a set of gemetric constraint or rules are called as layout design Rules.

→ The rules specify the minimum allowable line width for physical object on chip such as metal & polysilicon interconnection minimum allowable separation between two such features.

Example is if two lines are placed closed to each other it make short circuit in layout

→ the main, objectives of design rules is to achieve a high yied & reliability using smallest possible silicon & reliability using smallest possible silicon area.

→ There is usually a trade off between higher yield & better area efficiency

→ The layout design rules increases the probability of fabricating a successful product with high yield.

→ Usully design rules are of two types these are
(i) Micron Rules (μ-Rules)
(ii) Lamda Rules (λ Rules).

(i) Micron Rules (μ-Rules):

→ Then Rules in which the layout constraint such as minimum feature minimum allowable separation are stated in terms of absolute dimention in micrometer.

→ In micron Rules size is fixed

(ii) Lamda Rules (λ-Rules)

It specify the layout constraint in terms of parameter lamda & allow.

→ The design of layout is very tightly link to the performance such as speed, area, & power discipation. Physical structure directly determines the stray, conductance of transistor, parasitic capacitance & Resistance.

→ The mask layout design is process which starts from functionality, performance & specification of logic gate. Then it starts with circuit topology received diagram logic function. It estimate parasitic capacitance.

→ Then it codifies the sizing of to realized diagram performance specification. Then a simple stick diagram can be drawn by showing the location of contact.

→ After that a topologically visible layout is found. Mask layers are drawn according to the layout design rules.

→ After following design rules it goes for design Rule checking in which the circuit extraction procedure is performed on finish layout. Determine actual transistor size & parasitic capacitance of each node.
Then it goes for circuit simulation by using SPICE Technology to determine the performance of circuit.

→ If there is any fault in circuit & parasitic capacitance. Then it is goes for Resize & Modification after that we can able to get a complete layout design.

Stick diagram:-

→ It is a layout of showing location of transistors, local interconnection between the transistors & location of contact.

→ It is very difficult to find a Minimum area layout for complex c-mos logic circuit.

→ To avoide the drawback of layout design stick diagram is used.

→ To avoide the drawback of layout design stick diagram is used.

→ By the help of stick diagram we can minimize the ckt complexity can be reduced.

→ If we can minimize a no. of diffussion area both for n-mos & p-mos transistor spacing between poly silicon gates can be made smaller which is reduce the overall horizontal diamentions of circuit layout area.