GOVERNMENT POLYTECHNIC, DHENKANAL

LECTURE NOTES

Analog Electronics & OP-AMP

SEMESTER-6TH

PREPARED BY

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[CHAPTER-1]

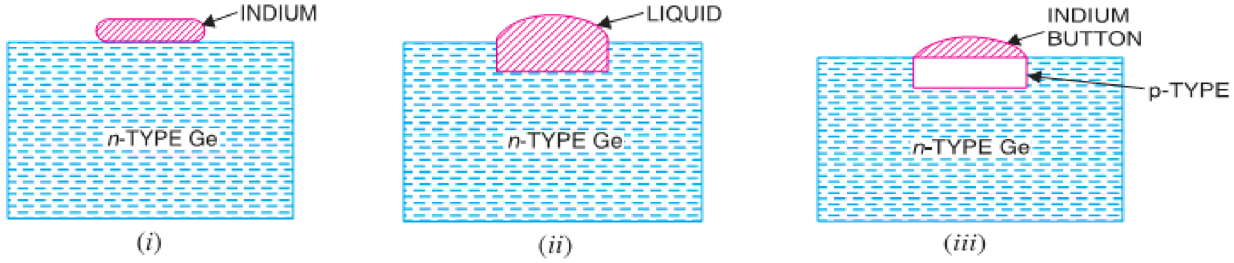
[DIODE & CIRCUITS]

CONSTRUCTION & WORKING PRINCIPLE OF DIODE: -

- When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called **PN Junction**. Most semiconductor devices contain one or more PN junctions.

Formation of PN junction.

- In actual practice, the characteristic properties of PN junction will not be apparent if a p-type block is just brought in contact with n-type block. In fact, it is **fabricated** by special techniques.
- There are a number of techniques for the fabrication of PN-Junction: -
  - Grown Junction
  - Alloy Junction
  - Diffused Junction
  - Epitaxial Growth
  - Point contract Junction.
- But the most common method of making PN junction is called **Alloying**.

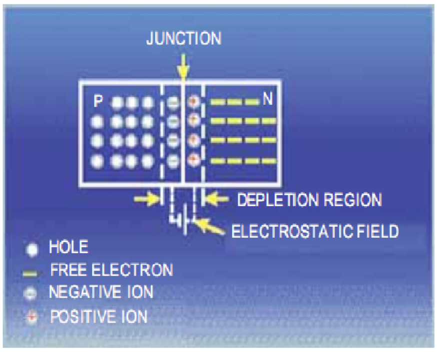


[Figures of different stages of formation of PN junction by Alloying method]

- In this method, a small block of indium (trivalent impurity) is placed on an n-type germanium slab as shown in Fig (i). The system is then heated to a temperature of about 500ºC.
- The indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture as shown in Fig (ii).
- The temperature is then lowered and puddle begins to solidify. Under proper conditions, the atoms of indium impurity will be suitably adjusted in the germanium slab to form a single crystal. Addition of indium overcomes the excess of electrons in the n-type germanium to such an extent that it creates a p-type region. As the process goes on, the remaining molten mixture becomes increasingly rich in indium.
- When all germanium has been redeposited, the remaining material appears as indium button which is frozen on to the outer surface of the crystallized portion as shown in Fig. (iii).

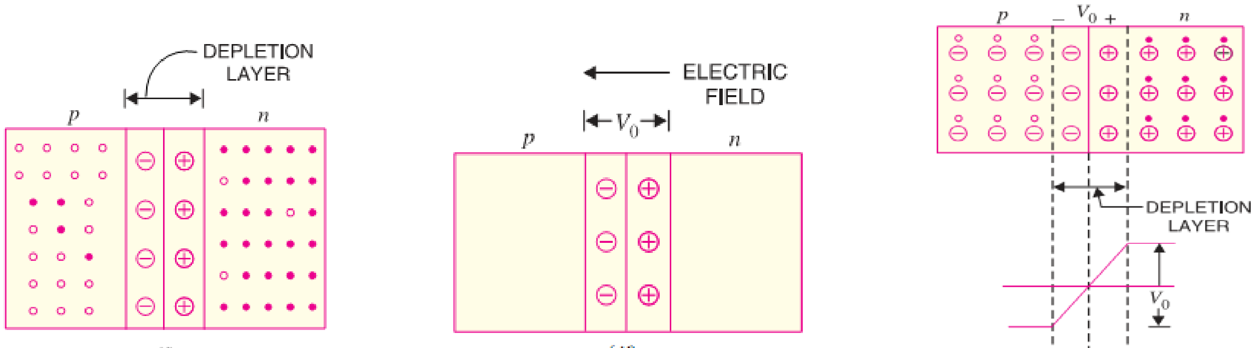
Properties of PN Junction.

- To explain PN junction, consider two types of materials: - 1) P-Type & 2) N-Type.
- P-type semiconductor having –ive acceptor ions and +ive charged holes. N-type semiconductor having +ive donor ions & –ive free electrons.
- P-type has high concentration of holes and N-type has high concentration of electrons.
- So there is a tendency for the free electron to diffuse over p-side and holes to n-side. This process is called **Diffusion.**
- When a free electron move across the junction from n-type to p-type, positive donor ions are removed by the force of electrons. Hence positive charge is built on the n-side of the junction.
- Similarly negative charge establish on p-side of the junction.
- When sufficient no of donor and accepter ions gathered at the junction, further diffusion prevented. Because +ive charge on n-side repel holes to cross from p-side to n-side, similarly –ive charge on p-side repel free electrons to cross from n-type to p-type.



- Thus a barrier is set up against further movement of charge carriers is hole or electrons. This barrier is called as **Potential Barrier/ Junction Barrier (V_0)** and is of the order 0.1 to 0.3 volt. This prevents the respective majority carriers for crossing the barrier region. This region is known as **Depletion Layer**

- The term depletion is due to the fact that near the junction, the region is depleted (i.e. emptied) of charge carries (free electrons and holes) due to diffusion across the junction.
- It may be noted that depletion layer is formed very quickly and is very thin compared to the n-region and the p-region.



(i) (ii)

- Once pn junction is formed and depletion layer created, the diffusion of free electrons stops. In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction. The positive and negative charges set up an electric field as shown in the fig above.
- The electric field is a barrier to the free electrons in the n-region. There exists a potential difference across the depletion layer and is called Barrier Potential (V_0).
- The barrier potential of a pn junction depends upon several factors including the type of semiconductor material, the amount of doping and temperature.
- The typical barrier potential is approximately: - For Silicon, $V_0 = 0.7$ V ; For Germanium, $V_0 = 0.3$ V

❖ <u>Junction Capacitance:-</u>

- When a PN junction is formed, a layer of positive and negative impurity ions is formed on either side of the pn junction. This depletion layer acts as dielectric (non-conductive) medium between P-region and N-region. Therefore, these regions act as two plates of a capacitor separated by dielectric medium.
- The capacitance formed in this junction is called as Depletion Layer Capacitance or Space Charge Capacitance or Transition Region Capacitance or simple **Junction Capacitance.**

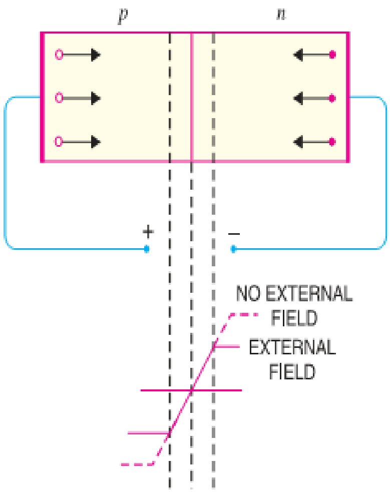
Applying D.C. Voltage Across PN Junction or Biasing a PN Junction

- In electronics, the term bias refers to the use of D.C. voltage to establish certain operating conditions for an electronic device. In relation to a PN junction, there are following two bias conditions :

1. Forward Biasing **2.** Reverse Biasing

❖ **<u>Forward Biasing</u>**. When external D.C. voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called **Forward Biasing**.

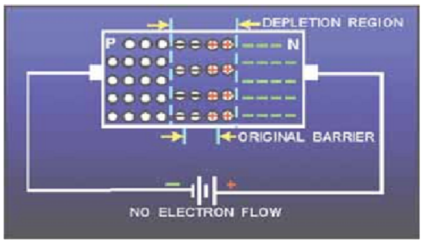
- To apply forward bias, connect positive terminal of the battery to p-type and negative terminal to n-type as shown in Fig.



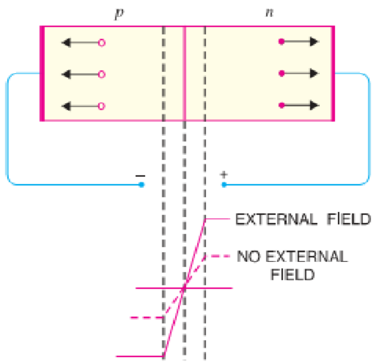
- The applied forward potential establishes an electric field which acts against the field due to potential barrier.
- Therefore, the resultant field is weakened and the barrier height is reduced at the junction.
- As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier.
- Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit.
- Thus, current flows in the circuit. This is called **Forward Current**.
- With forward bias to PN junction, the important points are: -

(i) The potential barrier is reduced and at some forward voltage i. e. (0.1 to 0.3 V), it is eliminated altogether.
(ii) The junction offers low resistance (forward resistance, R_f) to current flow.
(iii) Current flows in the circuit due to the establishment of low resistance path.
(iv) The magnitude of current depends upon the applied forward voltage.

❖ **Reverse Biasing.** When the external D.C. voltage applied to the junction is in such a direction that potential barrier is increased, it is called **Reverse Biasing.**



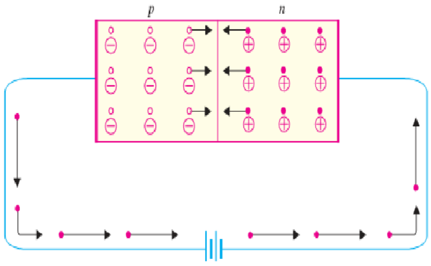
- For reverse bias, connect -ve terminal of battery to p-type and +ve terminal to n-type as shown in Fig.
- It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier.
- Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig.
- The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow.



♣ With reverse bias to PN junction, The important points are:
  (i) The potential barrier is increased.
  (ii) The junction offers very high resistance R_r) to current flow.
  (iii) No current flows in the circuit due to high resistance path.

- **Conclusion: -** From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs.
- Whereas with forward bias to junction low resistance path is set up & hence current flows in the circuit.

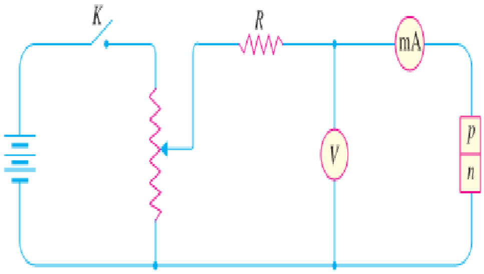
❖ **Current Flow in a Forward Biased PN Junction:-**



- It concluded that in n-type region, current carried by free electrons whereas in p-type region, it is carried by holes. However, in external connecting wires, current is carried only by free electrons.

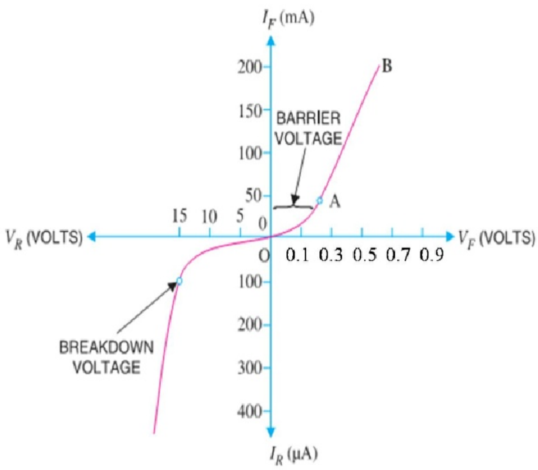
Volt-Ampere Characteristics of PN Junction:-

- Volt-ampere or V-I characteristic of a pn junction (also called a crystal or semiconductor diode) is the curve between voltage across the junction and the circuit current.
- Usually, voltage is taken along x-axis and current along y-axis. Fig. shows the circuit arrangement for determining the V-I characteristics of a pn junction.
- The characteristics can be studied under three heads, namely: - **(1)** Zero external voltage, **(2)** Forward Bias **(3)** Reverse Bias.



❖ **(i) Zero external voltage: -** When the external voltage is zero, i.e. circuit is open at K; the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point O in Fig.

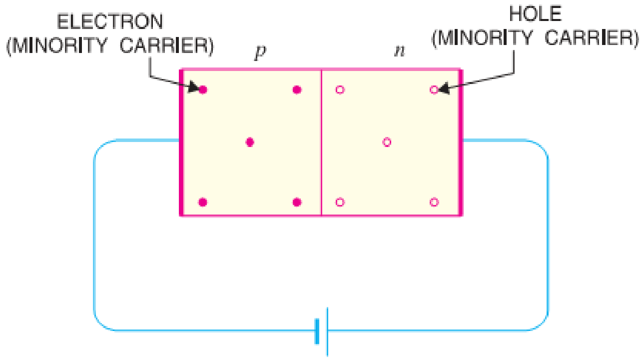
- **(ii) Forward Bias**: - With forward bias to the pn junction i.e. p-type connected to positive terminal and n-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage.
- Thus, a rising curve OB is obtained with forward bias as in Fig. From the forward characteristic, it is seen that at first (region OA), the current increases very slowly and the curve is non-linear. Because the external applied voltage is used up in overcoming the potential barrier.



- Once external voltage exceeds potential barrier voltage, the pn junction behaves like ordinary conductor.
- Therefore, the current rises very sharply with increase in external voltage (region AB on the curve). The curve is almost linear.

❖ **(iii) Reverse Bias: -** With reverse bias to the pn junction i.e. p-type connected to negative terminal and n-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit.

➢ However, in practice, a very small current (of the order of μA) flows in the circuit with reverse bias as shown in the reverse characteristic.



➢ This is called **Reverse Saturation Current** (Is) and is due to the minority carriers.

➢ It may be recalled that there are a few free electrons in p-type material and a few holes in n-type material.

➢ These undesirable free electrons in p-type and holes in n-type are called minority carriers. As shown in side Fig. to these minority carriers, the applied reverse bias appears as forward bias.

➢ Therefore, a small current flows in the reverse direction. If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms.

➢ At this stage breakdown of the junction occurs, characterized by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

➢ **Note: -**The forward current through a pn junction is due to the majority carriers produced by the impurity. However, reverse current is due to the minority carriers produced due to breaking of some co-valent bonds at room temperature.

❖ **Important Terms: -**

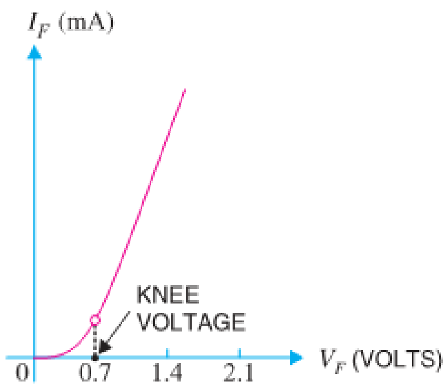
(i) Breakdown Voltage: - It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.

(ii) Knee Voltage: - The forward voltage at which the current through the junction starts to increase rapidly.

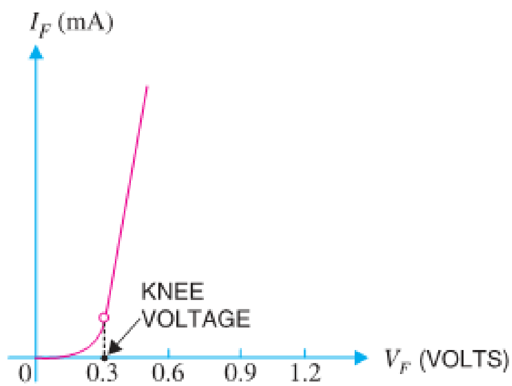
(iii) Peak inverse voltage (PIV):- It is the maximum reverse voltage that can be applied to the pn junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service.

(iv) Maximum forward current: - It is the highest instantaneous forward current that a pn junction can conduct without damage to the junction. Manufacturer's data sheet usually specifies this rating. If the forward current in a pn junction is more than this rating, the junction will be destroyed due to overheating.

(v) Maximum power rating: - It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction



SILICON



GERMANIUM

Other Type of DIODES: -

1.	Zener Diode	**2.**	Light Emitting Diode	**3.**	Tunnel Diode	**4.**	PIN Diodes
5.	Photo-Diode	**6.**	Varactor Diodes	**7.**	Laser Diodes	**8.**	Gunn Diodes
9.	Peltier diodes	**10.**	Step Recovery Diodes	**11.**	Schottky Diode	**12.**	Super Barrier Diodes
13.	Optoisolator	**14.**	Point-contact diodes	**15.**	Avalanche diodes	**16.**	Constant current diodes

DIODE CURRENT EQUATION: -

- The Mathematical equation, which describes the forward and reverse characteristics of a semiconductor diode is called the diode current equation.
- Let I = Forward or Reverse Diode Current,
  I_0 = Reverse Saturation Current
  V = External Voltage. (It is +Ve for Forward Bias, -Ve or Reverse Bias)
  η = A constant, whose value is equal to 1 for Ge diode and 2 for Si diode for relatively low value of diode current (i.e. at or below the knee of the curve) and ή = 1 for Ge & Si diode for higher levels of diode current. (i. e. in the rapidly increasing section of the curve)
  V_T =Volt-equivalent of temperature. Its value is given by the relation T/11,600, where T is the absolute temperature. At room temperature (i.e. 300K), V_T = 26vmV.
- The current equation for a forward biased diode is given by the relation,

$$\boxed{I = I_0 (e^{V/\eta \cdot V_T} - 1)}$$

We know that at room temperature, V_T = 26mV = 0.026V. Substituting the value of V_T in the above equation it becomes,

$$\boxed{I = I_0 (e^{40V/\eta} - 1)}$$

- Thus diode current at or below the knee of the curve for Germanium and Silicon is given by

$$\boxed{I_{Ge} = I_0 (e^{40V} - 1) \quad \textbf{[As } \eta\textbf{= 1 for Ge]}} \qquad \boxed{I_{Si} = I_0 (e^{20V} - 1) \quad \textbf{[As } \eta\textbf{= 1 for Si]}}$$

- If the value of applied voltage is greater than unity (i.e. for the diode current in the rapid by increasing section of the curve) then the equation of diode current for Germanium or Silicon is given by

$$\boxed{I = I_0 (e^{40V} - 1) \quad \textbf{[As } \eta\textbf{= 1 for Higher Value of Voltage]}}$$

- The current equation for a reverse biased diode may be obtained by changing the sign of the applied voltage (V), i.e.

$$\boxed{I = I_0 (e^{-V/\eta \cdot V_T} - 1)}$$

- If the Value of $V >> V_T$, then the term $-V/\eta \cdot V_T << 1$. Therefore $I = I_0$.
- Thus the diode current under reverse bias is equal to the reverse saturation current as long as the external voltage is below its break down value.

DIODE SPECIFICATION SHEET: -

- All manufactures of the semiconductor device provide data on specific diodes for the users to make proper utilization of the devices. This data could be a brief description limited to a one page or more than that. It includes the information arranged in table, graphs etc. The data is usually for : -
  - Forward voltage, V_F (At a specific Current & Temperature)
  - Maximum forward current, I_F (At a specific Temperature)
  - Reverse saturation current I_R or I_O (At a specific Voltage & Temperature)
  - Reverse Voltage Rating [PIV, PRV, VRRM or V(BR)], Where, BR=Breakdown at a specific current & temperature.
  - Maximum power dissipation level at a particular temperature.
  - Capacitance Value.
  - Reverse recovery time, t_{rr}.
  - Operating temperature range.
- Beside this, depending on the type of diode being considered, more data may also be provided such as frequency range, noise level, switching time, thermal resistance level and peak repetitive values.
- For the application in mind, the significance of the data will usually be self apparent.
- If the maximum power or dissipation rating is also provided, it is understood to be equal to the produce

$$P_{Dmax} = V_D I_D$$

Where I_D and V_D are the diode current and voltage at a particular point of operation.

DIODE APPLICATIONS:

- A PN junction diode has an important characteristic that it conducts well in forward direction and poorly in reverse direction. This characteristic makes a diode very useful in a number of applications given below:
  1. As Rectifiers or Power Diodes in D.C. power supply.
  2. As Signal Diodes in communication circuits.
  3. As Zener Diodes in voltage stabilizing circuits.
  4. As Varactor Diodes in radio and TV receivers.
  5. As a Switch in logic circuits used in computers

EFFECT OF TEMPERATURE OF DEPENDENCE OF JUNCTION DIODE:

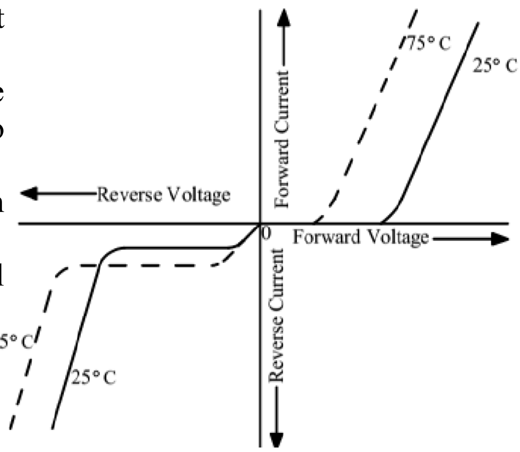
- We have already discussed in the last article that the diode current is a function of temperature and the temperature appears in the denominator of the exponent term of the diode current equation (i.e., $V/\eta \,.\, V_T$ is equal to T/11600).
- It is thus obvious that with the increase in temperature, the exponent will reduce and hence the diode current should also decrease.
- However, it has been found that the variation of saturation current (I_0) is much greater than the exponential term.
- The above fact may be expressed in the form of a mathematical relation as given below:

Let, I_{01} = Saturation current at temp (T_1) for Ge or Si diode,

& I_{02} = Saturation current at some other temperature (T_2)

Then

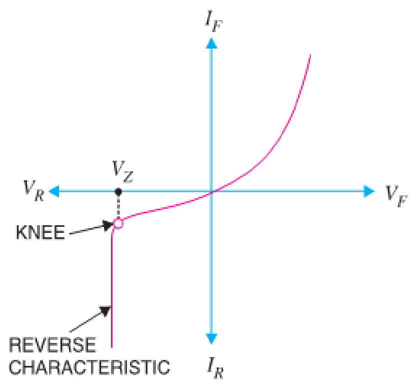
$$\boxed{I_{02} = I_{01} \,.\, 2^{(T2-T1)}/10}$$



- As discussed in last chapter the reverse saturation current (I_0) will be just about double in magnitude for every 10ºC increase in temperature.
- For example, a germanium diode with an I_0 in the order of 1 or 2μ A at 25ºC has a leakage current of 100μ A (= 0.1 mA) at a temperature of 100ºC.
- Current levels of this magnitude in the reverse bias region would certainly question our desired open-circuit condition in the reverse bias region.
- However, typical values of I_0 for silicon diode are much lower than that of germanium for similar power and current levels.
- The increasing level of I_0 with temperature account for the lower threshold voltage as shown in Fig.
- Due to this reason forward characteristic at 75ºC is shown to the left to that of the characteristic at 25ºC.
- As the temperature increases, the forward characteristic shifts more and more to the left of the characteristic at 25ºC (i.e. become more and more "ideal").
- However, temperature beyond the normal operating range can have a very detrimental effect on the diode's maximum power and current levels.
- We see in Fig., that in the reverse bias region, the breakdown voltage is increasing with the increase in temperature.

ZENER BREAK DOWN

- It has already been discussed that when the reverse bias on a crystal diode is increased, a critical voltage, called **Breakdown Voltage** is reached where the reverse current increases sharply to a high value.
- The breakdown region is the knee of the reverse characteristic as shown in Fig. The satisfactory explanation of this breakdown of the junction was first given by the American scientist C. Zener.
- The breakdown voltage is also called **Zener Voltage** or **Zener Break Down** & the sudden increase in current is known as **Zener Current**.

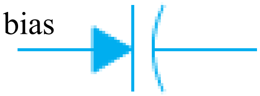


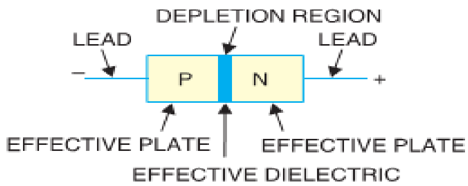
- The breakdown or Zener voltage depends upon the amount of doping.
- If the diode is heavily doped, depletion layer will be thin and consequently the breakdown of junction will occur at lower reverse voltage where as lightly doped diode has a higher breakdown voltage.

AVALANCHE BREAKDOWN: -

- In this case the increased reverse voltage increases the amount of energy imparted to minority carriers.
- As the reverse voltage is increased further the minority carriers acquires a large amount of energy.
- When these carriers collide with Si or Ge atoms, within the crystal structure, they impart sufficient energy to break a covalent bond and generate additional carriers (electron-hole pair).
- These additional carriers pick up energy from the applied voltage and generates still more carriers. As a result of this, the reverse current increases rapidly.
- This cumulative process of carrier generation (multiplication) is known as **Avalanche Break down** or Avalanche **Multiplication**

❖ VARACTOR DIODE

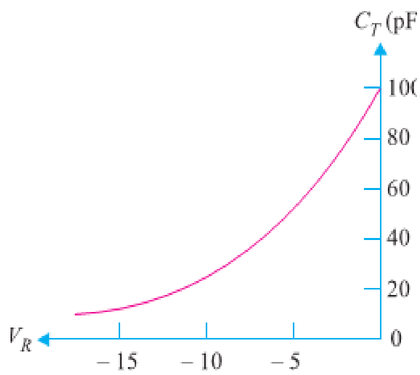
- A junction diode which acts as a variable capacitor under changing reverse bias  is known as a **varactor diode**. It is also known as **Varicap** or **Voltcap.**
- When a pn junction is formed, depletion layer is created in the junction area.
- Since there are no charge carriers within the depletion zone, the zone acts as an insulator.
- The p-type material with holes (+ive charge) as majority carriers and n-type material with electrons (−ive charge) as majority carriers act as charged plates.
- Thus the diode may be considered as a capacitor with n-region and p-region forming oppositely charged plates and with depletion zone between them acting as a dielectric.
- A varactor diode is specially constructed to have high capacitance under reverse bias.
- The values of capacitance of varactor diodes are in the pico farad (10^{-12} F) range.
- In normal operation, a varactor diode is always reverse biased.
- The capacitance of varactor diode is found as:



$$\boxed{C_T = \varepsilon\, A/W_d}$$

Where,

C_T = Total capacitance of the junction,
A = Cross-sectional area of the junction,
ε = Permittivity of the semiconductor material,
Wd = Width of the depletion layer.



- When reverse voltage across a varactor diode is increased, the width Wd of the depletion layer increases. Therefore, the total junction capacitance C_T of the junction decreases.
- On the other hand, if the reverse voltage across the diode is lowered, the width Wd of the depletion layer decreases. Consequently, the total junction capacitance C_T increases.
- It is used as **Voltage Variable Capacitor, Voltage-Controlled Tuning**

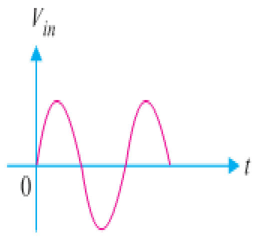
RECTIFIERS

❖ INTRODUCTION: -

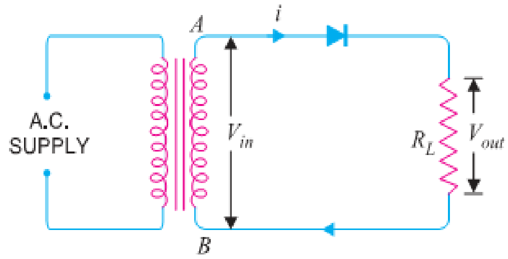
- For reasons associated with economics of generation and transmission, the electric power available is usually an A.C. Supply. The supply voltage varies sinusoidal and has a frequency of 50 Hz. It is used for lighting, heating and electric motors.
- But there are many applications (e.g. electronic circuits) where D.C. supply is needed. When such a D.C. Supply is required, the mains A.C. Supply is rectified by using *Crystal Diodes*.
- The following two rectifier circuits can be used: -
  - (i) Half-wave rectifier (ii) Full-wave rectifier

HALF-WAVE RECTIFIER:-

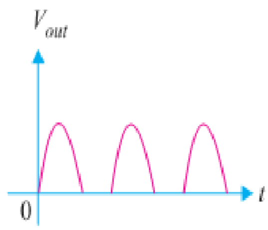
- In half-wave rectification, the rectifier conducts current only during the positive half-cycles of input A.C. Supply.
- The negative half-cycles of A.C. Supply is suppressed i.e. during negative half-cycles, no current is conducted and hence no voltage appears across the load.
- Therefore, current always flows in one direction through the load though after every half-cycle



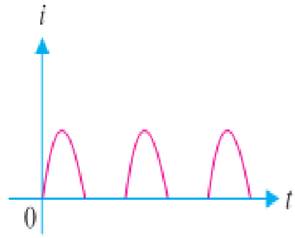
(Input Wave form)



(Half wave Rectifier Circuit)



(Output voltage wave)



(Output Current)

Circuit Details: -

- The above Fig shows the circuit where a single crystal diode acts as a half-wave rectifier.
- The A.C. Supply to be rectified is applied in series with the diode and load resistance R_L. Generally, A.C. Supply is given through a transformer.
- The *use of transformer* permits two advantages.
  - ✓ Firstly, it allows us to step up or step down the A.C. input voltage as the situation demands.
  - ✓ Secondly, the transformer isolates the rectifier circuit from power line and thus reduces the risk of electric shock.

OPERATION:-

- The A.C. voltage across the secondary winding AB changes polarities after every half-cycle.
- During the positive half-cycle of input A.C. voltage, end A becomes positive w.r.t. end B. This makes the diode forward biased and hence it conducts current.
- During the negative half-cycle, end A is negative w.r.t. end B. Under this condition, the diode is reverse biased and it conducts no current.
- Therefore, current flows through the diode during positive half-cycles of input A.C. voltage only; it is blocked during the negative half-cycles. In this way, current flows through load R_L always in the same direction. Hence D.C. output is obtained across R_L.
- It may be noted that output across the load is *pulsating D.C*. These pulsations in the output are further smoothened with the help of filter circuits discussed later.

Disadvantages : -

(i) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

(ii) The A.C. supply delivers power only half the time. Therefore, the output is low.

FULL-WAVE RECTIFIER: -

- In full-wave rectification, current flows through the load in the same direction for both half-cycles of input A.C. voltage. This can be achieved with two diodes working alternately.
- For the positive half- cycle of input voltage, one diode supplies current to the load and for the negative half-cycle, the other diode does so ; current being always in the same direction through the load.
- Therefore, a full-wave rectifier utilizes both half-cycles of input A.C. voltage to produce the D.C. output.
- The following two circuits are commonly used for full-wave rectification: -
  - **(i)** Centre-tap full-wave rectifier **(ii)** Full-wave bridge rectifier

CENTRE-TAP FULL-WAVE RECTIFIER:-

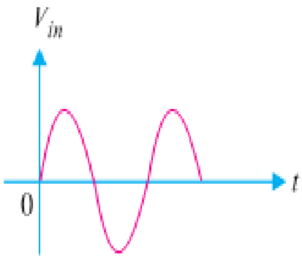
Circuit Details: -

- The circuit employs two diodes D_1 and D_2 as shown in Fig below. A centre tapped secondary winding AB is used with two diodes connected so that each uses one half-cycle of input A.C. voltage.
- In other words, diode D_1 utilizes the A.C. voltage appearing across the upper half (OA) of secondary winding for rectification while diode D_2 uses the lower half winding OB.

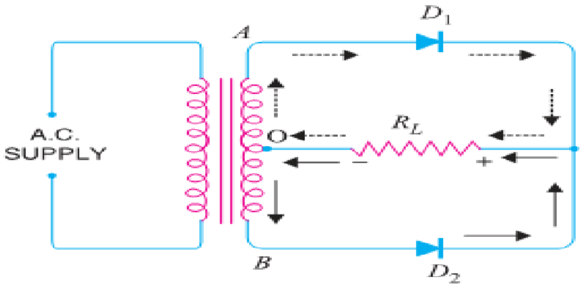
Circuit Operation: -

- During the positive half-cycle of secondary voltage, the end A of the secondary winding becomes positive and end B negative. This makes the diode D_1 forward biased and diode D_2 reverse biased.
- Therefore, diode D_1 conducts while diode D_2 does not. The conventional current flow is through diode D_1, load resistor R_L and the upper half of secondary winding as shown by the dotted arrows.
- During the negative half-cycle, end A of the secondary winding becomes negative and end B positive.

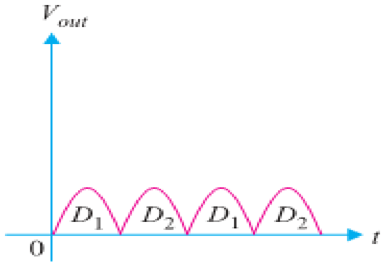
- Therefore, diode D_2 conducts while diode D_1 does not. The conventional current flow is through diode D_2, load R_L & lower half winding shown by solid arrows.
- It may be seen that current in the load R_L is in the same direction for both half-cycles of input A.C. voltage. Therefore, D.C. is obtained across the load R_L.



(Input Wave form)



(Centre-Tap Full-Wave Rectifier Circuit)



(Output wave form)

Advantages:-

(i) The D.C. output voltage and load current values are twice than that of a half wave rectifier.
(ii) The ripple factor is much less (0.482) than that of half rectifier (1.21).
(iii) The efficiency is twice (81.2%) than that of half wave rectifier (40.6%).

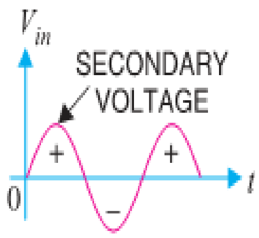
Disadvantages:-

(i) It is difficult to locate the centre tap on the secondary winding.
(ii) The D.C. output is small as each diode utilizes only one-half of the transformer secondary voltage.
(iii) The diodes used must have high peak inverse voltage.

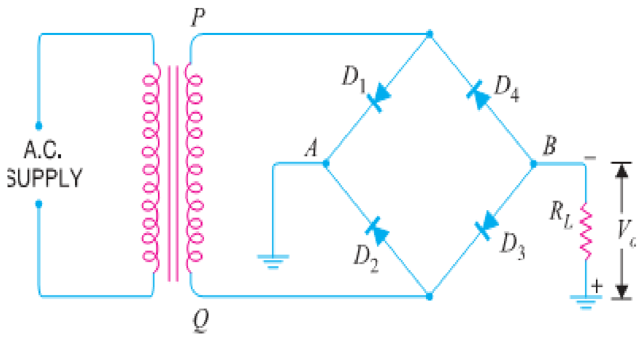
FULL-WAVE BRIDGE RECTIFIER: -

Circuit Details: -

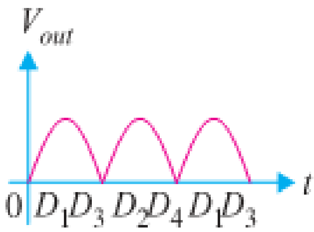
- The need for a centre tapped power transformer is eliminated in the bridge rectifier.
- It contains four diodes D_1, D_2, D_3 and D_4 connected to form bridge as shown in Fig below.
- The A.C. supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer.
- Between other two ends of the bridge, the load resistance R_L is connected.



(Input Wave Form)



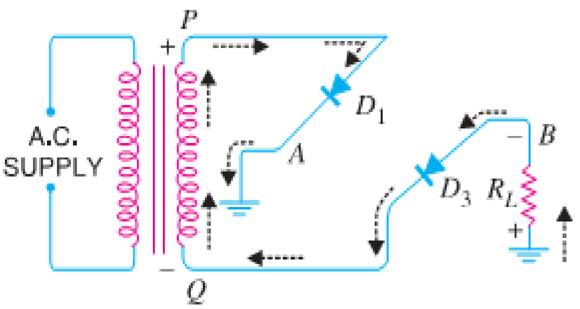
(Full-Wave Bridge Rectifier Circuit)

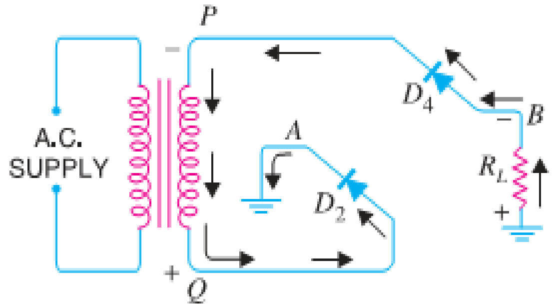


(Output wave form)

CIRCUIT OPERATION :-

- During the positive half-cycle of secondary voltage, the end P of the secondary winding becomes positive and end Q negative.
- This makes diodes D_1 and D_3 forward biased while diodes D2 and D4 are reverse biased.
- Therefore, only diodes D_1 and D_3 conduct. These two diodes will be in series through the load R_L as shown in Fig. below. The conventional current flow is shown by dotted arrows. It may be seen that current flows from A to B through the load R_L.
- During the negative half-cycle of secondary voltage, end P becomes negative and end Q positive. This makes diodes D_2 and D_4 forward biased whereas diodes D_1 and D_3 are reverse biased.
- Therefore, only diodes D_2 and D_4 conduct. These two diodes will be in series through the load R_L as shown in Fig. below. The current flow is shown by the solid arrows.
- It may be seen that again current flows from A to B through the load i.e. in the same direction as for the positive half-cycle. Hence, D.C. output is obtained across load R_L.





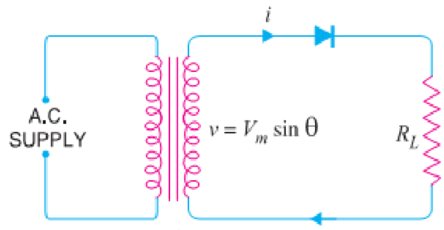
(Full-Wave Bridge Rectifier Circuit in +ve Half Cycle) (Full-Wave Bridge Rectifier Circuit -ve Half Cycle)

- **Advantages: -**
  (i) The need for centre-tapped transformer is eliminated.
  (ii) The output is twice that of the centre-tap circuit for the same secondary voltage.
  (iii) The PIV is one-half that of the centre-tap circuit (for same D.C. output).
- **Disadvantages: -**
  (i) It requires four diodes. (ii) Internal resistances high.

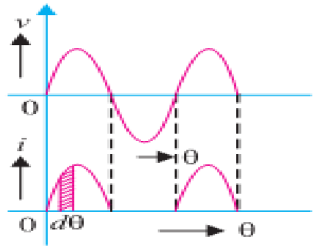
Mathematical Derivation for Rectification Efficiency for HALF WAVE rectifier : -

- The ratio of d.c. power output to the applied input a.c. power is known as rectifier efficiency i.e.,

$$\text{Rectifier efficiency, } \eta = \frac{\text{d.c. power output}}{\text{Input a.c. power}}$$



- Consider a half-wave rectifier shown in Fig.
- Let v = $V_m \sin\theta$ be the alternating voltage that appears across the secondary winding. Let r_f and R_L be the diode resistance and load resistance respectively.
- The diode conducts during positive half-cycles of a.c. supply while no current conduction takes place during negative half-cycles.



OUTPUT D.C. POWER :-

- The output current is pulsating direct current. Therefore, in order to find D.C. power, average current has to be found out.

$$\text{Average Value} = \frac{\text{Area Under The Curve Over a cycle}}{\text{Base}} = \int_0^{\pi} \frac{i\,d\theta}{2\pi}$$

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\,d\theta = \frac{1}{2\pi}\int_0^{\pi}\frac{V_m \sin\theta}{rf + R_L}\,d\theta = \frac{V_m}{2\pi(rf+R_L)}\int_0^{\pi}\sin\theta\,d\theta = \frac{V_m \sin\theta}{rf+R_L}[-\cos\theta]_0^{\pi}$$

$$= \frac{V_m}{2\pi(rf+R_L)} \times [(-\cos\pi) - (-\cos 0)] = \frac{V_m}{2\pi(rf+R_L)} \times 2 = \frac{V_m}{(rf+R_L)} \times \frac{1}{\pi} = \frac{I_m}{\pi} \quad [\because I_m = \frac{V_m}{(rf+R_L)}]$$

$\therefore$ D.C. Power, $\mathbf{P_{dc}} = I_{dc}^2 \times R_L = (\frac{I_m}{\pi}^2) \times R_L$

INPUT A.C. POWER: -

- The A.C. power input is given by : $P_{ac} = I_{rms}^2(rf + R_L)$ For a half-wave rectified wave, $\mathbf{I_{rms} = I_m/2}$

$\therefore$ $\mathbf{P_{ac}} = (\frac{I_m}{2})^2 \times (rf + R_L)$

$$\therefore \quad \text{Rectifier efficiency} = \frac{\text{d.c.output power}}{\text{a.c.input power}} = \left(\frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2\,(rf+R_L)}\right) = \frac{0.406\,R_L}{rf+R_L} = \frac{0.406\,R_L}{1+\frac{rf}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ **Max. Rectifier Efficiency for HALF WAVE Rectifier = 40.6%**

- It shows that in half-wave rectification, a maximum of 40.6% of a. c. power is converted into d. c. power.

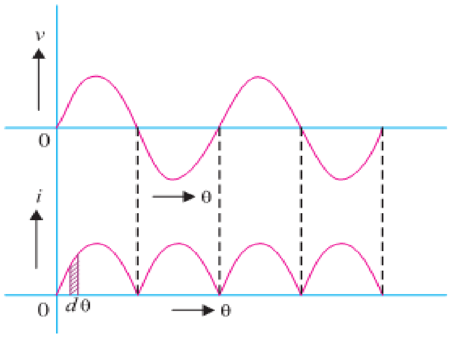
NOTE: - $I_{rms} = [\frac{1}{2\pi}\int_0^{2\pi} i^2\,d\theta]^{½} = [\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\theta\,d\theta + \frac{1}{2\pi}\int_{\pi}^{2\pi} 0\,d\theta]^{½} = [\frac{I_m^2}{2\pi}\int_0^{\pi}\frac{1-\cos 2\theta}{2}\,d\theta]^{½}$

$$= [\frac{I_m^2}{4\pi}[\theta - \frac{\sin 2\theta}{2}]_0^{\pi}]^{½} = [\frac{I_m^2}{4\pi}[\pi - 0 - \frac{\sin 2\pi}{2} + \sin 0]]^{½} = [\frac{I_m^2}{4\pi} \times \pi]^{½} = [\frac{I_m^2}{4}]^{½} = \frac{I_m}{2} \rightarrow \mathbf{I_{rms}} = \frac{I_m}{2}$$

Similarly, $\mathbf{V_{rms} = V_m/2}$ for Half Wave and For Full Wave Rectifier $\mathbf{I_{rms} = I_m/\sqrt{2}}$ and $\mathbf{V_{rms} = V_m/\sqrt{2}}$

Mathematical Derivation for Rectification Efficiency for FULL WAVE Rectifier : -

- Fig. shows the process of full-wave rectification.
- Let $v = V_m \sin\theta$ be the a.c. voltage to be rectified. Let rf and R_L be the diode resistance and load resistance respectively.
- Obviously, the rectifier will conduct current through the load in the same direction for both half-cycles of input a.c. voltage. The instantaneous current *i* is given by :



$$i = \frac{v}{(rf + R_L)} = \frac{V_m \sin\theta}{(rf + R_L)}$$

D.C. OUTPUT POWER.

- The output current is pulsating direct current. Therefore, in order to find the d.c. power, average current has to be found out. For a full wave rectifier the average value or dc value can be found like half wave ,

$$I_{dc} = \frac{2I_m}{\pi}$$

$\therefore$ D.C. power output, $P_{dc} = I_{dc}^2 \times R_L = (\frac{2I_m}{\pi})^2 \times R_L$

A.C. INPUT POWER.

- The a.c. input power is given by :

$$P_{ac} = I_{rms}^2 (rf + R_L)$$

For a full-wave rectified wave, we have, $I_{rms} = I_m/\sqrt{2}$

$$\therefore \quad P_{ac} = (\frac{I_m}{\sqrt{2}})^2 (rf + R_L)$$

$\therefore$ Full-wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{(\frac{I_m}{\sqrt{2}})^2 (rf + R_L)} = \frac{8}{\pi^2} \times \frac{R_L}{(rf + R_L)} = \frac{0.812\, R_L}{rf + R_L} = \frac{0.812}{1 + \frac{rf}{R_L}}$$

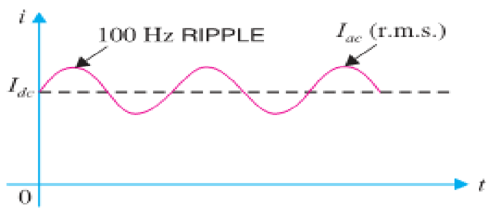
The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Maximum efficiency = 81.2%

- This is double the efficiency due to half-wave rectifier. Therefore, a full-wave rectifier is twice as effective as a half-wave rectifier.

RIPPLE FACTOR: -

- The output of a rectifier consists of a d.c. component and an a.c. component (also known as ripple).
- The a.c. component is undesirable and accounts for the pulsations in the rectifier output.
- The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output; the smaller this component, the more effective is the rectifier.
- Ripple mean unwanted ac signal present in the rectified output.



- The ratio of R.M.S. value of A.C. component to the D.C. component in the rectifier output is known as *ripple factor* i.e.

$$\text{Ripple factor} = \frac{\text{r.m.s. value of a.c component}}{\text{value of d.c. component}} = \frac{I_{ac}}{I_{dc}}$$

Mathematical Analysis.

- The output current of a rectifier contains d.c. as well as a.c. component.
- By definition, the effective (i.e. r.m.s.) value of total load current is given by :

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2} \quad \text{Or} \quad I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

- Dividing throughout by I_{dc}, we get,

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2}$$ (But I_{ac}/ I_{dc} is the ripple factor.)

$$\therefore \quad \text{Ripple factor} = \frac{1}{I_{dc}} \sqrt{I_{rms}^2 - I_{dc}^2} = \sqrt{(\frac{I_{rms}}{I_{dc}})^2 - 1}$$

(i) **For half-wave rectification: -**

In half-wave rectification, $I_{rms} = I_m/2$; $I_{dc} = I_m/\pi$

$\therefore$ Ripple factor $= \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = 1.21$

- It is clear that a.c. component exceeds the d.c. component in the output of a half-wave rectifier.
- This results in greater pulsations in the output.
- Therefore, half-wave rectifier is ineffective for conversion of a.c. into d.c.

(ii) **For full-wave rectification**: -

In full-wave rectification, $I_{rms} = \frac{I_m}{\sqrt{2}}$; $I_{dc} = \frac{2I_m}{\pi}$

$\therefore$ Ripple factor $= \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = 0.48$ i.e. $\frac{\text{effective a.c. component}}{\text{d.c. component}} = 0.48$

- This shows that in the output of a full-wave rectifier, the d.c. component is more than the a.c. component. Consequently, the pulsations in the output will be less than in half-wave rectifier.
- For this reason, full-wave rectification is invariably used for conversion of a.c. into d.c.

Peak Inverse Voltage (PIV) : -

- The maximum value of reverse voltage occurs at the peak of the input cycle, which is equal to V_m.
- This maximum reverse voltage is called peak inverse voltage (PIV). Thus the PIV of diode : -

a) For Half Wave = V_m, **b)** For Center Tapped $= 2V_m$ and **c)** For Bridge Rectifier = V_m.

Transformer Utilization Factor (TUF) : -

- It may be defined as the ratio of d.c. power delivered to the load and the a.c. rating of the transformer secondary.

Thus, $\boxed{\mathbf{TUF = P_{dc} / P_{ac}}}$

- For half wave rectifier, TUF = **0.287**; Center taped rectifier, TUF = **0.693**; Bridge rectifier, TUF **= 0.812**.
- The TUF is very useful in determining the rating of a transformer to be used with rectifier circuit.

Average Value of Voltage & Current for HALF WAVE Rectifiers: -

- If V_m= Maximum value of the a.c. input voltage, then the average or d.c. value of the output voltage and current is given by

$$\boxed{\mathbf{V_{dc} = V_m/\pi = 0.318\ V_m \quad \text{and} \quad I_{dc} = I_m/\pi = 0.318\ I_m}}$$

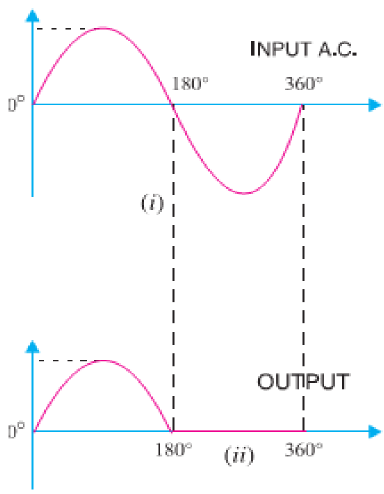
Average Value of Voltage & Current for FULL WAVE Rectifiers: -

- If V_m= Maximum value of the a.c. input voltage, then the average or d.c. value of the output voltage and current is given by

$$\boxed{\mathbf{V_{dc} = 2V_m/\pi = 0.636\ V_m \quad \text{and} \quad I_{dc} = 2I_m/\pi = 0.636\ I_m}}$$

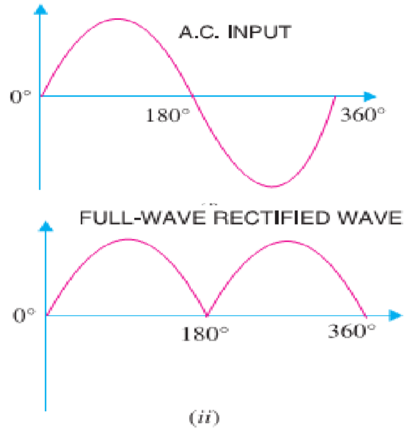
Output Frequency of Half Wave Rectifier: -

- The output frequency of a half-wave rectifier is equal to the input frequency (50 Hz). Recall how a complete cycle is defined.



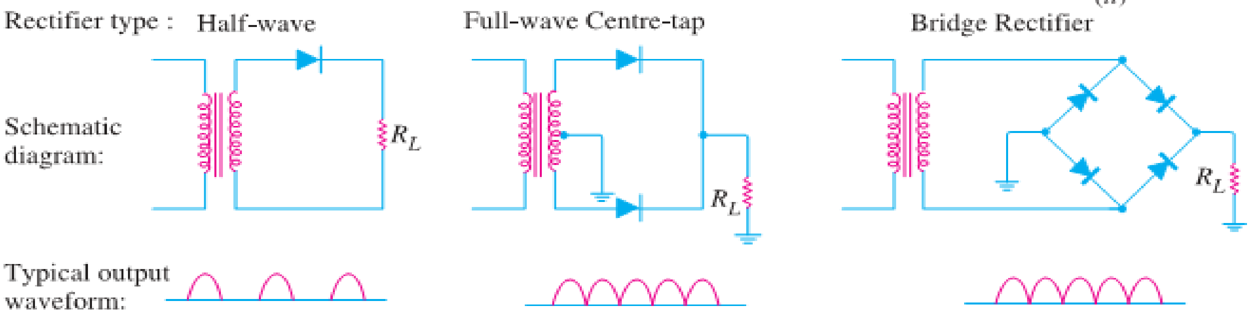
- A waveform has a complete cycle when it repeats the same wave pattern over a given time.
- Thus in Fig. (i), the a.c. input voltage repeats the same wave pattern over 0° – 360°, 360° – 720° and so on.
- In Fig. (ii), the output waveform also repeats the same wave pattern over 0° – 360°, 360° – 720° and so on.
- This means that when input a.c. completes one cycle, the output half wave rectified wave also completes one cycle.
- In other words, for the half wave rectifier the output frequency is equal to the input frequency i.e. $\mathbf{f_{out} = f_{in}}$
- For example, if the input frequency of sine wave applied to a half-wave rectifier is 100 Hz, then frequency of the output wave will also be 100 Hz.

Output Frequency of Full Wave Rectifier: -



- The output frequency of a full-wave rectifier is double the input frequency.
- As a wave has a complete cycle when it repeats the same pattern.
- In Fig. (i), the input a.c. completes one cycle from 0° – 360°.
- However, in Fig. (ii) full-wave rectified wave completes two cycles in this period.
- Therefore, output frequency is twice the input frequency i.e. $\mathbf{f_{out} = 2f_{in}}$
- For example, if the input frequency to a full-wave rectifier is 100 Hz, then the output frequency will be 200 Hz.

COMPARISON OF RECTIFIERS: -



S. No.	Particulars	Half-wave	Centre-tap	Bridge type
1	No. of diodes	1	2	4
2	Transformer necessary	no	yes	no
3	Max. efficiency	40.6%	81.2%	81.2%
4	Ripple factor	1.21	0.48	0.48
5	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
6	Peak inverse voltage	V_m	$2V_m$	V_m

FILTER CIRCUITS:-

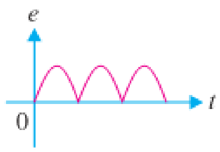
- Generally, a rectifier is required to produce pure D.C. supply for using at various places in the electronic circuits.
- However, the output of a rectifier has pulsating character i.e. it contains A.C. and D.C. components.
- The A.C. component is undesirable and must be kept away from the load.
- To do so, a filter circuit is used which removes (or filters out) the A.C. component and allows only the D.C. component to reach the load.
- A **filter circuit** is a device which removes the A.C. component of rectifier output but allows the D.C. component to reach the load.
- A filter circuit is generally a combination of inductors (L) and capacitors (C).
- The filtering action of L and C depends upon the basic electrical principles.
- A capacitor offers infinite reactance to d.c.
- We Know that $X_C = 1/2\pi fC$. But for D.C., f = 0.

  ∴ $X_C = 1/2\pi fC = 1/2\pi \times 0 \times C = \infty$ (Means Capacitor shows *infinite reactance* to DC)

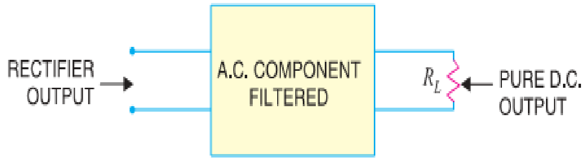
  ♣ ***Hence, a Capacitor does not allow d.c. to pass through it.***
- We know $X_L = 2\pi fL$. For d.c., f = 0

  ∴ $X_L = 2\pi \times 0 \times L = 0$ (Means Inductor shows *zero reactance* to DC)

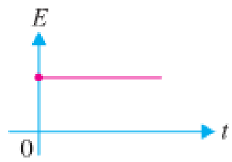
  ♣ ***Hence Inductor passes d.c. quite readily.***
- *A Capacitor passes A.C. but does not pass D.C. at all. On the other hand, an Inductor opposes A.C. but allows D.C. to pass through it.*
- It then becomes clear that suitable network of L and C can effectively remove the A.C. component, allowing the D.C. component to reach the load.



(Pulsating D.C)



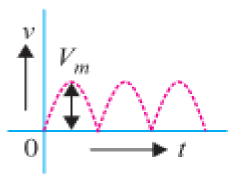
(Filter Circuit)



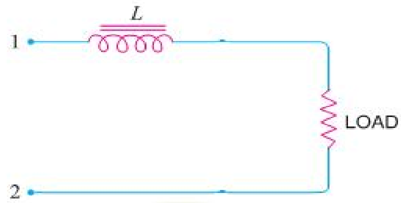
(Pure D.C)

- **Types Of Filter Circuits:-**
- There are different types of filter circuits according to their construction. The most commonly used filter circuits are : -
  - *Inductive Filter or Series Inductor,*
  - *Capacitor Filter or Shunt Capacitor*,
  - *Choke Input Filter or LC Filter* and
  - *Capacitor Input Filter* or *π-Filter*.

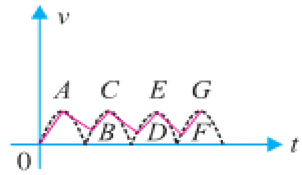
✓ **Inductive Filter Or Series Inductor:-**



(Rectified output Pulsating d.c)



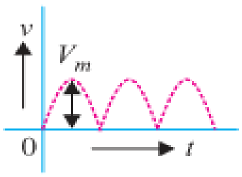
(Inductive Filter Circuit)



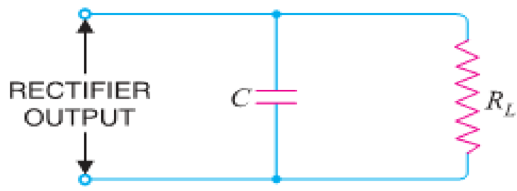
(Output of Inductive Filter)

- Fig. (ii) Shows a typical Inductive filter circuit. It consists of an Inductor L placed across the rectifier output in series with load R_L.
- The choke (Inductor with iron core) offers high opposition to the passage of a.c. component but no opposition to the d.c. component.
- The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at Load resistance R_L.

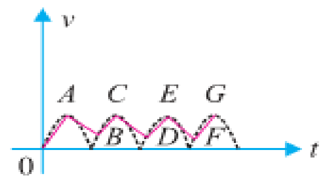
✓ **Capacitor Filter Or Shunt Capacitor:-**



(Rectified output Pulsating d.c)



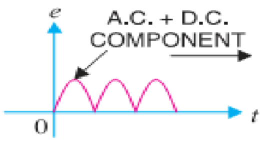
(Capacitor Filter Circuit)

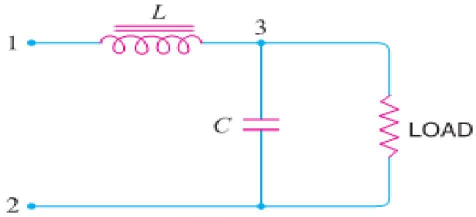


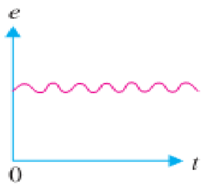
(Output of Capacitor Filter)

- Fig. (ii) Shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L.
- The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load.
- At the end of quarter cycle [Point A in Fig. (iii)], the capacitor is charged to the peak value V_m of the rectifier voltage.
- Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it decreases as shown by the line AB in Fig. (iii).
- The voltage across load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor.
- This process is repeated again and again and the output voltage waveform becomes ABCDEFG. It may be seen that very little ripple is left in the output.
- Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.
- The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics.

✓ Choke Input Filter Or LC Filter:-



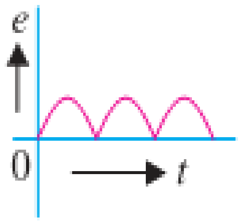


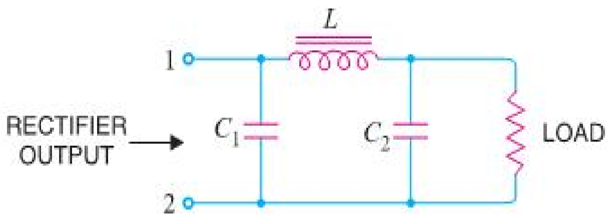


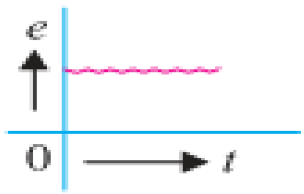
(Rectified output Pulsating d.c) (Choke Input Filter Circuit) (Output of Choke Input Filter)

- Fig. shows a typical choke input filter circuit. It consists of a choke L connected in series with the rectifier output and a filter capacitor C across the load.
- Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.
- The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit.
- As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component.
- The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.
- At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke.
- Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load.
- In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

✓ Capacitor Input Filter or π-Filter:-







(Rectified output Pulsating d.c) (Capacitor Input or π- Filter Circuit) (Output of π-Filter)

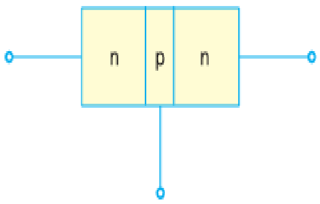
- Fig. shows a typical capacitor input filter or π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke Lin series and another filter capacitor C_2 connected across the load.
- Only one filter section is shown but several identical sections are often used to improve the smoothing action. The pulsating output from the rectifier is applied across the input terminals (i.e. terminals 1 & 2) of the filter.
- The filtering action of the three components viz C_1 , L and C_2 of this filter is described below :
  (a) The **filter capacitor C_1** offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.
  (b) The **choke L** offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the un bypassed a.c. component is blocked.
  (c) The **filter capacitor C_2** bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire

[CHAPTER-2]

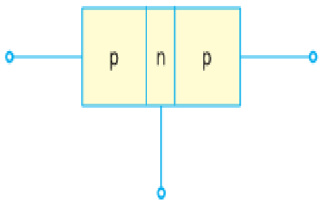
[TRANSISTORS AND CIRCUIT ANALYSIS]

❖ INTRODUCTION:-

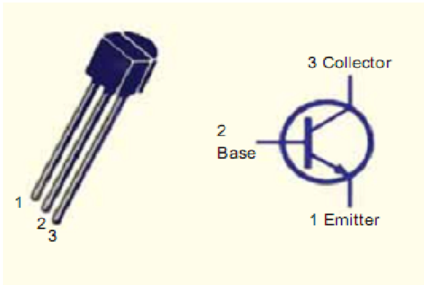
- When a third doped element is added to a crystal diode in such a way that two PN junctions are formed, the resulting device is known as a **Transistor**.
- This is a new type of electronics device which can able to amplify a weak signal in a fashion comparable and often superior to that realized by vacuum tubes.
- A transistor consists of two PN junctions formed by sandwiching either p-type or n-type semiconductor between a pair of opposite types. Hence Transistor is classified into two types, namely: -
    - **(i)** n-p-n transistor **(ii)** p-n-p transistor
- An n-p-n transistor is composed of two n-type semiconductors separated by a thin section of p-type.
- However, a p-n-p transistor is formed by two p-sections separated by a thin section of n-type as shown in Figure below.



(i)



(ii)



❖ NAMING: -

- A transistor has *two pn junctions*. As discussed later, one junction is forward biased and the other is reverse biased.
- The *forward biased junction* has a low resistance path whereas a *reverse biased junction* has a high resistance path.
- The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor transfers a signal from a low resistance to high resistance.
- The prefix '**trans**' means the signal transfer property of the device while '**istor**' classifies it as a solid element in the same general family with resistors.

❖ NAMING THE TRANSISTOR TERMINALS:-

- A transistor (PNP or NPN) has three sections of doped semiconductors.
- The section on one side is the **emitter** and the section on the opposite side is the **collector**.
- The middle section is called the **base** and forms two junctions between the emitter and collector.

(i)Emitter: -

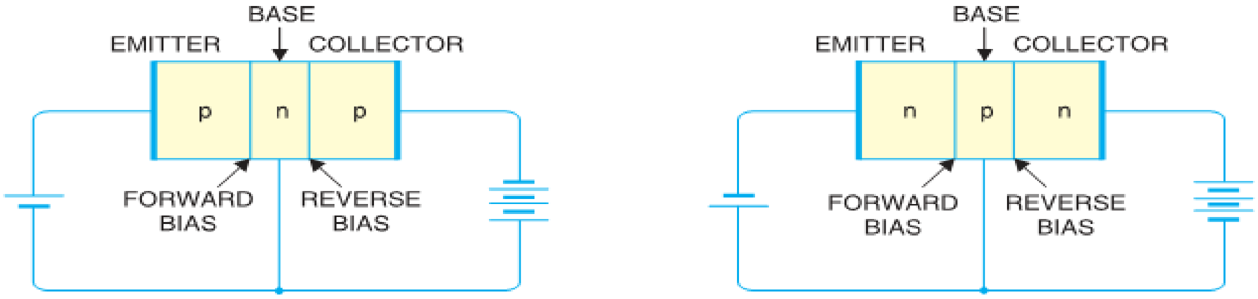
- The section on one side that *supplies charge carriers* (electrons or holes) is called the emitter.
- The emitter is always forward biased w.r.t. base so that it can supply a large number of majority carriers.
- The emitter (p-type) of PNP transistor is forward biased and supplies hole charges to its junction with the base. Similarly the emitter (n-type) of NPN transistor has a forward bias and supplies free electrons to its junction with the base.

(ii) Collector: -

- The section on the other side that *collects the charges* is called the collector. The collector is always reverse biased. Its function is to remove charges from its junction with the base.
- The collector (p-type) of PNP transistor has a reverse bias and receives hole charges that flow in the output circuit. Similarly the collector (n-type) of NPN transistor has reverse bias & receives electrons.

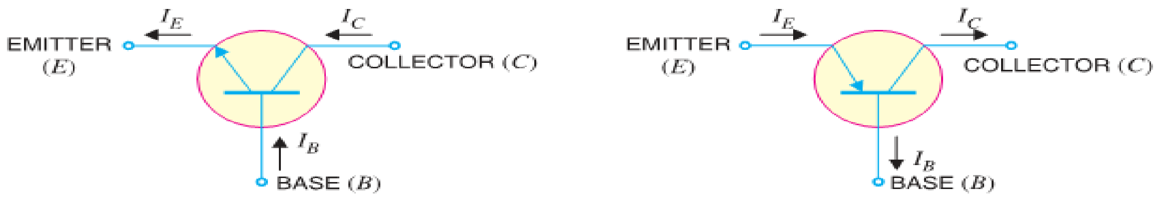
(iii)Base: -

- The middle section which forms two PN-junctions between emitter & collector is called base.
- The base-emitter junction is forward biased, allowing low resistance for the emitter circuit.
- The base-collector junction is reverse biased and provides high resistance in the collector circuit.



(i) (ii)

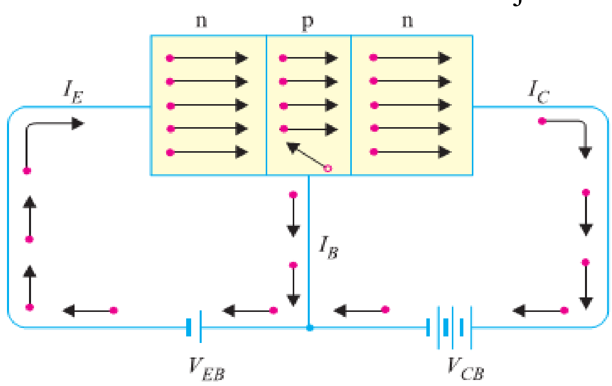
❖ **TRANSISTOR SYMBOL:-**



(i) (ii)

❖ **<u>WORKING OF NPN TRANSISTOR (NPN): -</u>**

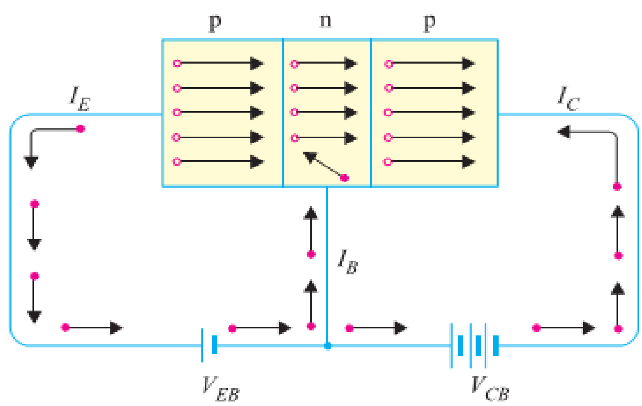
- The NPN transistor with forward bias to emitter- base junction & reverse bias to collector-base junction.
- The forward bias causes the electrons in the n-type emitter to flow towards the base.
- This constitutes the emitter current $\mathbf{I_E}$. As these electrons flow through the p-type base, they tend to combine with holes.
- As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base current $\mathbf{I_B}$.
- The remainders (more than 95%) cross over into the collector region to constitute collector current $\mathbf{I_C}$.



- In this way, almost the entire emitter current flows in the collector circuit.
- It is clear that emitter current is the sum of collector and base currents i.e. $\mathbf{I_E = I_B + I_C}$

❖ **<u>WORKING OF PNP TRANSISTOR (PNP): -</u>**

- Fig. shows the basic connection of a PNP transistor.
- The forward bias causes the holes in the p-type emitter to flow towards the base.
- This constitutes the emitter current I_E.
- As these holes cross into n-type base, they tend to combine with the electrons.
- As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C.



- In this way, almost the entire emitter current flows in the collector circuit.
- It may be noted that current conduction within PNP transistor is by holes. However, in the external connecting wires, the current is still by electrons

❖ TRANSISTOR CONNECTIONS:-

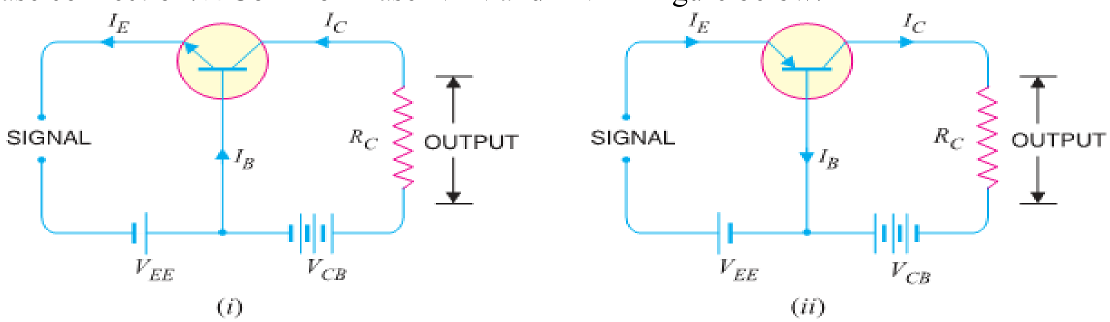
- There are three leads in a transistor such as emitter, base and collector terminals.
- However, when a transistor is to be connected in a circuit, we require **four terminals**; two for the input and two for the output.
- This difficulty is overcome by making one terminal of it in common to both input and output terminals.
- The input is fed between this common terminal and one of the other two terminals.
- The output is obtained between the common terminal and the remaining terminal.
- So a transistor can be connected in a circuit in the following ways:-

  (i) Common Base connection **(ii)** Common Emitter connection **(iii)** Common Collector connection

(i)Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from collector and base.

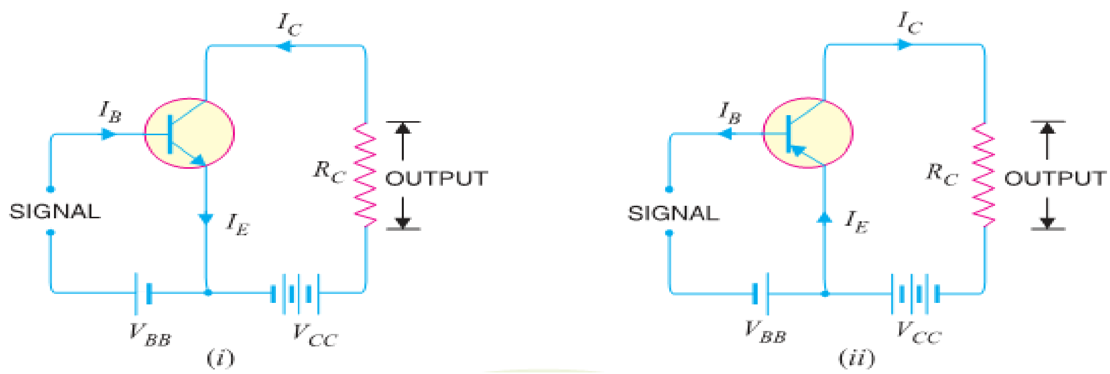
Here, base of the transistor is common to both input and output circuits and hence the name **C**ommon **B**ase connection. A Common Base NPN and PNP in figure below.



(ii) Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter.

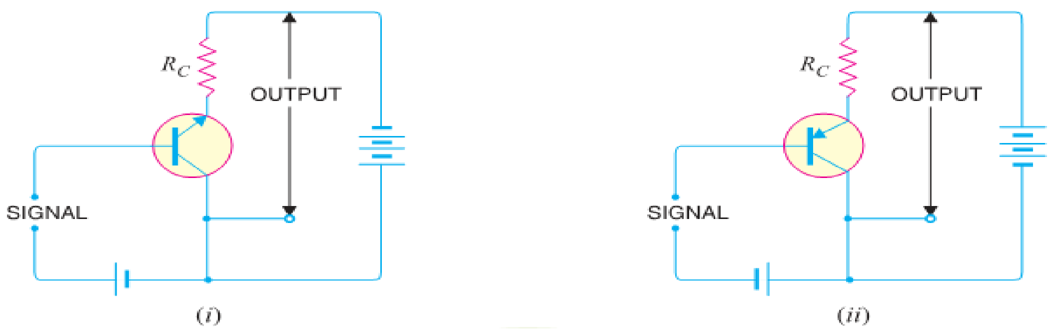
Here, emitter of the transistor is common to both input and output circuits and hence the name **C**ommon **E**mitter connection. A Common Emitter NPN and PNP transistor circuit is shown in figure below.



(iii) Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector.

Here, collector of the transistor is common to both input and output circuits and hence the name **C**ommon **C**ollector connection. A Common Collector NPN and PNP in figure below.



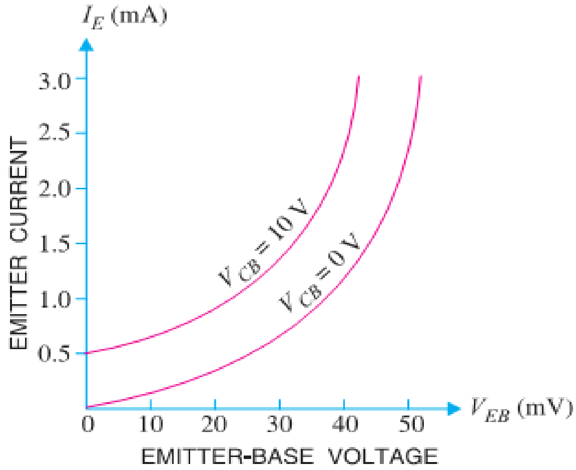
❖ TRANSISTOR CHARACTERISTICS:-

1) Characteristics of Common Base Connection

- The complete electrical behavior of a transistor can be described by stating the interrelation of the various currents and voltages.
- These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor.
- The most important characteristics of common base connection are **input characteristics** and **output characteristics**.

A) **Input Characteristics:-**

- It is the curve between emitter current $\mathbf{I_E}$ & emitter-base voltage $\mathbf{V_{BE}}$ at constant collector-base voltage $\mathbf{V_{CB}}$.
- The emitter current is generally taken along y-axis and emitter-base voltage along x-axis. Fig. Shows the input characteristics of a typical transistor in CB arrangement.



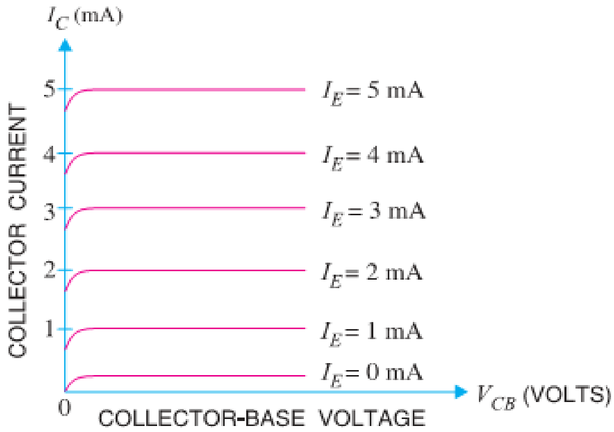
- The following points may be noted from these characteristics :
  - ♣ The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.
  - ♣ The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.
- **Input Resistance: -** It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) i.e.

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$

- In fact, input resistance is the opposition offered to the signal current. As a very small V_{EB} is sufficient to produce a large flow of emitter current I_E, thus, input resistance is quite small, of the order of a few ohms.

B) **Output Characteristics:-**

- It is the curve between collector current $\mathbf{I_C}$ & collector-base voltage $\mathbf{V_{BC}}$ at constant emitter current $\mathbf{I_E}$.
- Generally, collector current is taken along y-axis and collector-base voltage along x-axis.
- The fig. shows the input and output characteristics of a typical transistor in CB arrangement.
- The following points may be noted from characteristics :



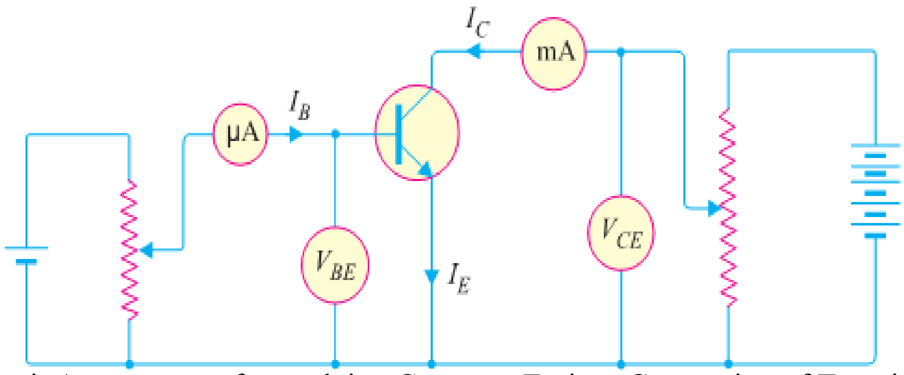
  - ♣ The collector current I_C varies with V_{CB} only at very low voltages (< 1V). The transistor is never operated in this region.
  - ♣ When the value of V_{CB} is raised above 1 − 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows almost entirely to the collector terminal. The transistor is always operated in this region.
  - ♣ A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.
- **Output Resistance**: - It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current i.e.

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

- The output resistance of CB circuit is very high, of the order of several tens of kilo-ohms.

2) Characteristics of Common Emitter Connection:-

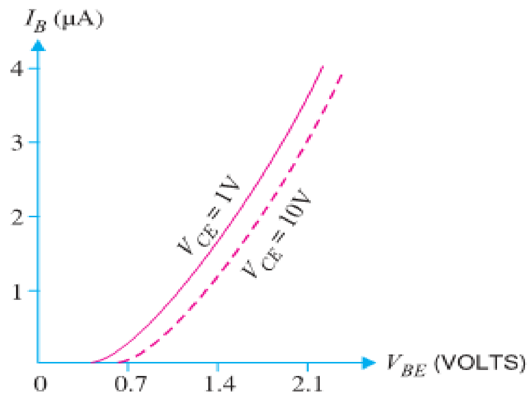
- The important characteristics of this circuit arrangement are the input characteristic and output characteristic.



(Circuit Arrangement for studying Common Emitter Connection of Transistor)

A) Input Characteristics:-

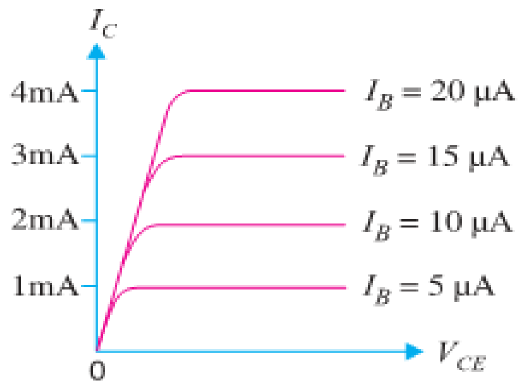
- It is the curve between base current IB & base-emitter voltage VBE at constant collector-emitter volt V_{CE}. The input characteristics of a CE connection can be determined by the circuit shown in Fig. Keeping V_{CE} constant (Let 10 V), note the base current I_B for various values of V_{BE}.



- Then plot the readings obtained on the graph, taking I_B along y-axis and V_{BE} along x-axis. This gives the input characteristic at V_{CE} = 10V as shown in Fig.
- The following points may be noted from the characteristics :
  - The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.
  - As compared to CB arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a CE circuit is higher than that of CB circuit.
- **Input Resistance: -** It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE}. The value of input resistance for CE circuit is of the order of a few hundred ohms

B) Output Characteristics: -

- It is the curve between collector current $\mathbf{I_C}$ and collector-emitter voltage $\mathbf{V_{CE}}$ at constant base current $\mathbf{I_B}$.
- The output characteristics of CE circuit can be drawn with the help of above circuit arrangement in Fig.
- Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for various values of V_{CE}.



- Then plot the readings on a graph, taking I_C along y-axis and V_{CE} along x-axis.
- This gives the output characteristic at I_B = 5 μA as shown in Fig. The test can be repeated for I_B= 10 μA to obtain the new output characteristic as shown in Fig.
- Following similar procedure, a family of output characteristics can be drawn as shown in Fig.
- The following points may be noted from the characteristics:
  - (i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, I_C becomes almost constant & independent of V_{CE}. This value of V_{CE} upto which I_C changes with V_{CE} is called the knee voltage (V_{knee}). The transistors are always operated in the region above knee voltage.
  - (ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.
  - (iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$
- **Output Resistance: -** It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B i.e.

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

- ➢ It may be noted that whereas the output characteristics of CB circuit are horizontal, they have noticeable slope for the CE circuit.
- ➢ Therefore, output resistance of CE circuit is less than that of CB circuit. Its value is of the order of 50 kΩ.

3) Characteristics of Common Collector Connection:-

- In a Common Collector circuit connection the load resistor connected from emitter to ground, so the collector tied to ground even though the transistor is connected in a manner similar to the CE connection.
- Hence there is no need for a set of common-collector characteristic to choose the parameters of the circuit. The output characteristic of the CC configuration is same as CE configuration.
- For CC Connection the output characteristic are plot of $\mathbf{I_E}$ **versus** $\mathbf{V_{CE}}$ for a constant value of $\mathbf{I_B}$.
- There is an almost unnoticeable change in the vertical scale of I_C of the CE connection if I_C is replaced by I_E for CC connection. The input circuit of CC connection, the CE characteristic is sufficient to obtain the required information.
- Hence Common Collector circuit connection is known as **Emitter Follower**.

❖ <u>CURRENT AMPLIFICATION FACTORS</u>: - (It is the ratio of output current to input current)

1) Common Base Connection:-

In a common base connection, the input current is the Emitter Current $\mathbf{I_E}$ and output current is the Collector Current $\mathbf{I_C}$.

Hence the ratio of change in collector current to the change in emitter current at constant collector-base voltage V_{CB} is known as current amplification factor for CB Connection and is denoted as **α (Alpha).**

$$\boxed{\alpha = \frac{\Delta I_C}{\Delta I_E}}$$

- ♣ Practical values of α in commercial transistors range from 0.9 to 0.99.

2) Common Emitter Connection:-

In a common emitter connection, the input current is the Base Current $\mathbf{I_B}$ and output current is the Collector Current $\mathbf{I_C}$.

Hence ratio of change in collector current (I_C) to the change in base current (I_B) at constant collector-emitter voltage V_{CE} is known as current amplification factor for CE Connection and denoted as **β (Beta).**

$$\boxed{\beta = \frac{\Delta I_C}{\Delta I_B}}$$

- ♣ Usually, its value ranges from 20 to 500.

3) Common Collector Connection:-

In a common collector connection, the input current is the Emitter Current $\mathbf{I_B}$ and output current is the Emitter Current $\mathbf{I_E}$.

Hence the ratio of change in emitter current to the change in base current at constant V_{CC} is known as current amplification factor for CC Connection and is denoted as **γ (Gamma).**

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

- ♣ This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \approx \Delta I_C$.

❖ RELATION AMONG DIFFERENT CURRENT AMPLIFICATION FACTORS:-

$$\boxed{\Delta I_E = \Delta I_B + \Delta I_C}$$

1) Relation between α and β :-

- ♣ As, $\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{1-\Delta I_C/\Delta I_E} = \frac{\alpha}{1-\alpha}$ ➔ As, $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{1+\Delta I_C/\Delta I_B} = \frac{\beta}{1+\beta}$

2) Relation between α and γ :-

- ♣ As, $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\Delta I_B/\Delta I_E}{1-\Delta I_C/\Delta I_B} = \frac{1}{1-\alpha}$ ➔ As, $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_E - \Delta I_B}{\Delta I_E} = \frac{\Delta I_E/\Delta I_B - 1}{\Delta I_E/\Delta I_B} = \frac{\gamma-1}{\gamma}$

3) Relation between β and γ :-

- ♣ As, $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_B + \Delta I_C}{\Delta I_B} = \frac{\Delta I_B}{\Delta I_B} + \frac{\Delta I_C}{\Delta I_B} = 1 + \beta$ ➔ As, $\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_B} - \frac{\Delta I_B}{\Delta I_B} = \gamma - 1$

4) Relation between α, β and γ:-

- ♣ As, $\beta = \frac{\alpha}{1-\alpha} = \alpha \text{ X } \frac{1}{1-\alpha} = \alpha \times \gamma$

$$\boxed{\therefore \beta = \alpha \text{ X } \gamma}$$

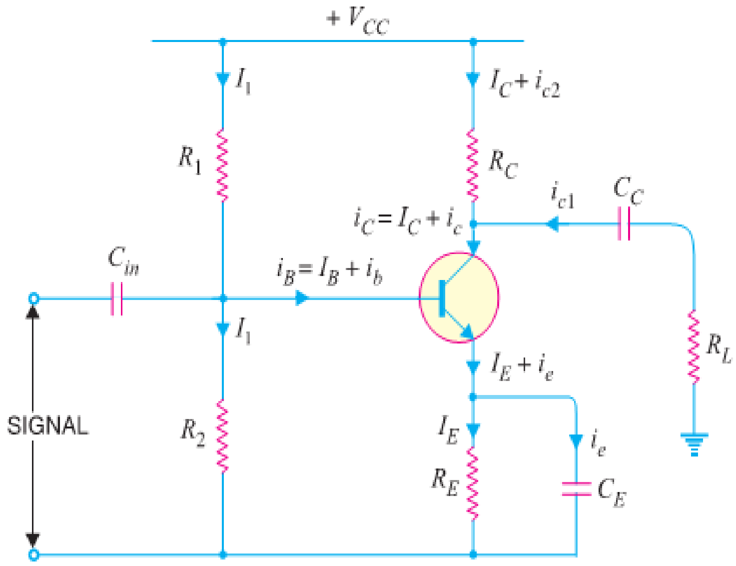
$\boxed{\therefore \alpha = \frac{\beta}{1+\beta}}$ $\boxed{\therefore \beta = \frac{\alpha}{1-\alpha}}$ $\boxed{\therefore \gamma = \frac{1}{1-\alpha}}$ $\boxed{\therefore \quad \gamma-1}$ $\boxed{\therefore \gamma = 1+\beta}$ $\boxed{\therefore \beta = \gamma + 1}$

♣ COMPARISON OF TRANSISTOR CONNECTIONS:-

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

- Out of the three transistor connections, the **Common Emitter Circuit** is the most efficient.
- It is used in about 90 to 95 per cent of all transistor applications.
- The main reasons for the widespread use of this circuit arrangement are :
  (i) High current gain. (ii) High voltage and power gain. (iii) Moderate output to input impedance ratio.

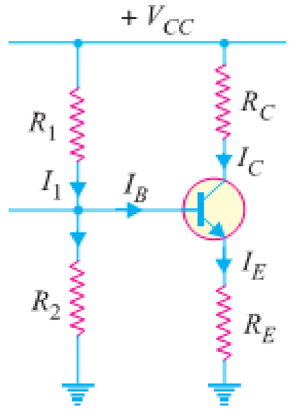
❖ D.C. AND A.C. EQUIVALENT CIRCUITS: -



- Various circuit currents. It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig.
- **(i) Base Current: -** When no signal is applied in the base circuit, D.C. base current I_B flows due to biasing circuit. When A.C. signal is applied, A.C. base current i_b also flows.
- Therefore, with the application of signal, Total Base Current i_B is given by: $\mathbf{i_B = I_B + i_b}$
- **(ii) Collector Current: -** When no signal is applied, a D.C. collector current I_C flows due to biasing circuit. When A.C. signal is applied, A.C. collector current i_c also flows.
- Therefore, the Total Collector Current i_C is given by: - $\mathbf{i_C = I_C + i_c}$

  Where $I_C = \beta\, I_B$ = zero signal collector current and $i_c = \beta\, i_b$ = collector current due to signal.
- **(iii) Emitter Current:-** When no signal is applied, a D.C. emitter current I_E flows. When A.C. signal is applied, A.C. Emitter Current i_e also flows. Therefore the Total Emitter Current is : - $\mathbf{i_E = I_E + i_e}$
- It is useful to keep in mind that: $I_E = I_B + I_C$ and $i_e = i_b + i_c$.
- But base current is usually very small, therefore, as a reasonable approximation, $I_E \approx I_C$ and $i_e \approx i_c$.

❖ **D. C. Equivalent Circuit: -** In order to draw the equivalent D.C. circuit, the following two steps are applied to the transistor circuit:-
  (a) Reduce all A.C. sources to zero.
  (b) Open all the capacitors.



- Referring D.C. Equivalent Circuit

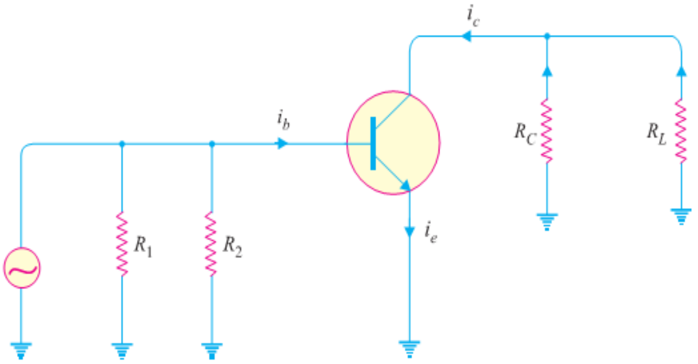
  D.C. Load $\mathbf{R_{DC} = R_C + R_E}$ & $V_{CC} = V_{CE} + I_C\,(R_C + R_E)$
- The maximum value of V_{CE} will occur when there is no collector current i.e. $I_C = 0$.

$$\therefore \quad \boxed{\textbf{Maximum } V_{CE} = V_{CC}}$$

- The maximum collector current will flow when $V_{CE} = 0$.

$$\therefore \quad \boxed{\textbf{Maximum } I_C = V_{CC}/\,(R_C + R_E)}$$

❖ **A.C. Equivalent Circuit: -** In order to draw A.C. equivalent circuit, the following two steps are applied to the transistor circuit:
(a) Reduce all D.C. sources to zero (i.e. $V_{CC}= 0$).
(b) Short all the capacitors.



- Referring A.C. Equivalent circuit A.C. load equal to $R_C \parallel R_L$ i.e. A.C. load, $\mathbf{R_{AC} = (R_C R_L/ (R_C+R_L)}$
- Maximum positive swing of A.C. collector-emitter voltage = $I_C \times R_AC$

∴ Total maximum **collector-emitter voltage,** $\mathbf{V_{CE\ MAX} = V_{CE}+ I_C R_{AC}}$

- Maximum positive swing of A.C. collector current = V_{CE}/R_{AC}

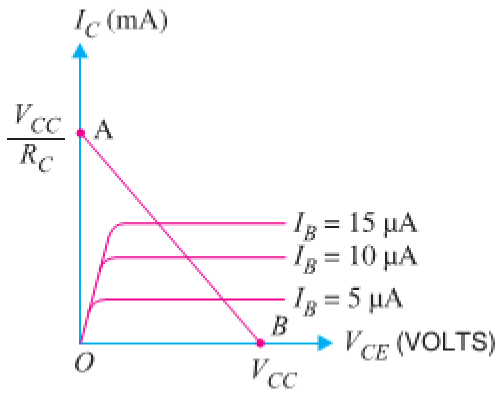
∴ Total maximum **collector current,** $\mathbf{I_{C\ MAX} = I_C+ V_{CE}/R_{AC}}$

❖ LOAD LINE ANALYSIS: -

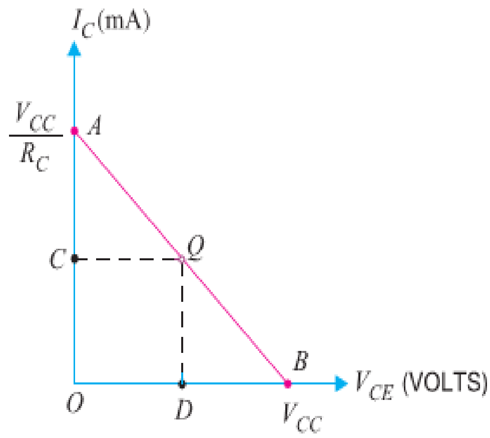
- In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages.
- One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as **load line method** can be used to solve such problems.
- This method is quite easy and is frequently used in the analysis of transistor applications.

♣ **D.C. LOAD LINE**: - It is the line on the output characteristics of a transistor circuit which gives the values of I_C and V_{CE} corresponding to zero signal or D.C. conditions.

- Consider a common emitter NPN transistor circuit where no signal is applied. Therefore, D.C. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig.

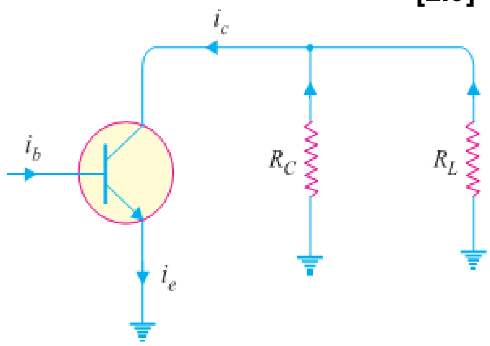


- The value of collector-emitter voltage V_{CE} at any time is given by ; $V_{CE} = V_{CC} - I_C R_C$ Or $I_C R_C = V_{CC} - V_{CE}$
  Or $I_C = V_{CC}/ R_C - V_{CE}/ R_C$
  Or $I_C = (-1/ R_C) V_{CE} + V_{CC}/ R_C$ (≡ Y= mX + C)
- As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as **D.C. Load Line.**
- To add load line, we need two end points of the straight line. These two points can be located as under:
  (i) When the collector current $I_C= 0$, then collector-emitter voltage is maximum and is equal to V_{CC}
  i.e. Max. $V_{CE}= V_{CC}- I_C R_C = V_{CC}$ (As $I_C = 0$)
- This gives the first point B (OB $=V_{CC}$) on the collector-emitter voltage axis as shown in Fig.
  (ii) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC}/R_C
  i.e. $V_{CE}= V_{CC}- I_C R_C$ or $0 = V_{CC}- I_C R_C$
  ∴ Max. $I_C= V_{CC}/R_C$

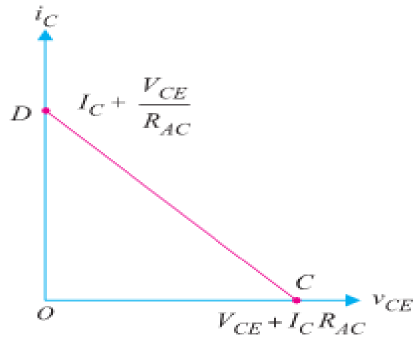


- This gives the second point A (OA $=V_{CC}/R_C$) on the collector current axis as shown in Fig.
- By joining these two points, **D.C. Load Line** AB is constructed.

♣ **(II) A.C. LOAD LINE.** This is the line on the output characteristics of a transistor circuit which gives the values of i_C and v_{CE} when signal is applied.



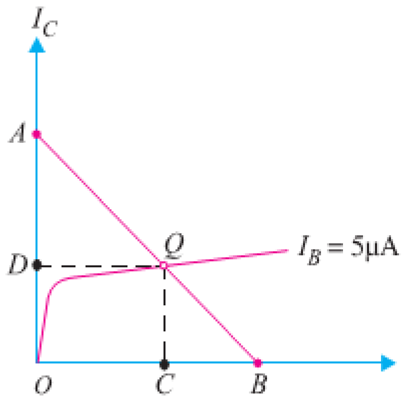
- Referring back to the transistor amplifier shown in Fig., its A.C. equivalent circuit as far as output circuit is concerned is as shown in Fig.
- To add A.C. load line to the output characteristics, we again require two end points: –
  1. One maximum collector-emitter voltage point **($V_{CE\ MAX}$)** and
  2. Other is maximum collector current point. **($I_{C\ MAX}$)**



- Under the application of A.C. signal, these values are Maximum collector-emitter voltage, $\mathbf{V_{CE\ MAX} = V_{CE} + I_C R_{AC}}$.
- This locates the point C of the A.C. load line on the collector-emitter voltage axis.
- Maximum collector current, $\mathbf{I_{C\ MAX} = I_C + V_{CE}/R_{AC}}$
- This locates the point D of A.C. load line on the collector-current axis.
- By joining points C and D, the **A.C. Load Line** CD is constructed.

❖ OPERATING POINT: -

- The zero signal values of I_C and V_{CE} are known as the **Operating point**.
- It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied.

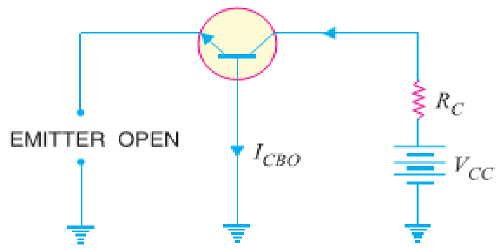


- It is also called quiescent (silent) point or **Q-Point** because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent i.e. in the absence of the signal.
- Suppose in the absence of signal, the base current is 5μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on $I_B = 5\ \mu A$ characteristic.
- But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d. c. load line AB.
- The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig, for $I_B = 5\ \mu A$, the zero signal values are :

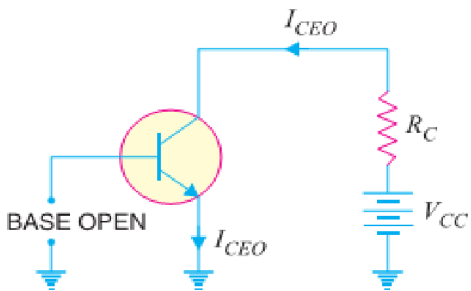
$$V_{CE} = OC \text{ volts} \qquad I_C = OD \text{ mA}$$

- It follows, therefore, that the zero signal values of I_C and V_{CE} (i.e. operating point) are determined by the point where d.c. load line intersects at proper base current curve.

❖ THE LEAKAGE CURRENT:-



- The current is due to the movement of minority carriers is known as Leakage Current.
- In Common Base Connection of Transistor the leakage current $\mathbf{I_{CBO}}$ is the Collector-Base current with emitter open.
- Similarly, In Common Emitter Connection the leakage current $\mathbf{I_{CEO}}$ is the Collector-Emitter Current with open Base.



- Expression for collector current in Common Base Connection is given by,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

- Expression for collector current in Common Emitter Connection is given by,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \quad \text{Or} \quad I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

❖ FAITHFUL AMPLIFICATION :-

✍ The process of raising the strength of a weak signal without any change in its general shape is known as *Faithful Amplification*. The key factor for achieving faithful amplification: -

- ♣ (i) Proper zero signal collector current
- ♣ (ii) Minimum proper base-emitter voltage (V_{BE}) at any instant
- ♣ (iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant

❖ TRANSISTOR BIASING: -

✍ The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as *Transistor Biasing*.

✍ The following are the most commonly used methods of obtaining transistor biasing from one source of supply (i.e. V_{CC}):

- ♣ (i) Base Resistor Method
- ♣ (ii) Emitter Bias Method
- ♣ (iii) Biasing with Collector-Feedback Resistor
- ♣ (iv) Voltage-Divider Bias.

❖ STABILISATION: -

✍ The process of making operating point independent of temperature changes or variations in transistor parameters is known as *Stabilization*.

❖ NEED FOR STABILIZATION:-

Stabilization of the operating point is necessary due to the following reasons :

- ♣ (i) Temperature dependence of IC
- ♣ (ii) Individual variations
- ♣ (iii) Thermal runaway

✍ The self-destruction of an unsterilized transistor is known as ***Thermal Runaway***.

❖ STABILITY FACTOR :-

✍ The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} [= I_{CEO}] at constant β and I_B is called stability factor i.e.

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

❖ SIMPLE PROBLEMS ON TRANSISTOR: -

1. In a common base connection, I_E = 1mA, I_C = 0.95mA. Calculate the value of I_B.

Solution: Using the relation, $I_E = I_B + I_C$

Or $1 = I_B + 0.95$ ∴ $I_B = 1 - 0.95 =$ **0.05 mA**

2. In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Solution: Here, $\alpha = 0.9$, $I_E = 1$ mA

Now $\alpha = \frac{I_C}{I_E}$ Or $I_C = \alpha I_E = 0.9 \times 1 = 0.9$ mA

Also $I_E = I_B + I_C$ ∴ Base current, $I_B = I_E - I_C = 1 - 0.9 =$ **0.1 mA**

3. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current. Given that α= 0.92.

Solution: Here, $I_E = 1$ mA, $\alpha = 0.92$, $I_{CBO} = 50$ μA

∴ Total collector current, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3} = 0.92 + 0.05 =$ **0.97 mA**

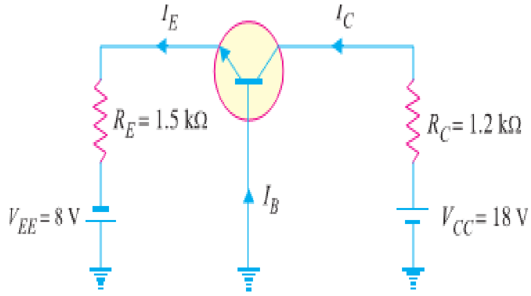
4. In a common base connection, α= 0.95. The voltage drop across 2 kΩ resistance which is connected in the collector is 2V. Find the base current.

Solution: The voltage drop across R_C (= 2 kΩ) is 2V. ∴ $I_C = 2\text{ V}/2\text{ k}\Omega = 1$ mA

Now $\alpha = I_C/I_E$ ∴ $I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05$ mA

Using the relation, $I_E = I_B + I_C$ ∴ $I_B = I_E - I_C = 1.05 - 1 =$ **0.05 mA**

5. For the common base circuit shown in Fig. determine I_C & V_{CB}. Assume the transistor is Silicon.



Solution: Since the transistor is of silicon, $V_{BE} = 0.7V$.

Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

Or $$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{8V - 0.7V}{1.5\ K\Omega} = 4.87\ mA$$

$\therefore$ $I_C \approx I_E =$ **4.87 mA**

Applying Kirchhoff's voltage law to the collector-side loop, we have,

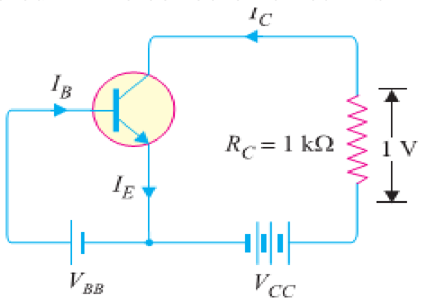
$V_{CC} = I_C R_C + V_{CB}$ ➔ $V_{CB} = V_{CC} - I_C R_C =$ 18 V − 4.87 mA × 1.2 kΩ = **12.16 V**

6. Calculate I_E in a transistor for which β= 50 and I_B = 20 μA.

Solution: Here β = 50, I_B = 20μA = 0.02 mA

Now $\beta = \frac{I_C}{I_B}$ $\therefore$ $I_C = \beta I_B = 50 \times 0.02 = 1$ mA ; Using the relation, $I_E = I_B + I_C = 0.02 + 1 =$ **1.02mA**

7. For a transistor, β = 45 and voltage drop across 1kΩ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.



Solution: Fig. shows the required common emitter connection.

The voltage drop across R_C (= 1 kΩ) is 1volt.

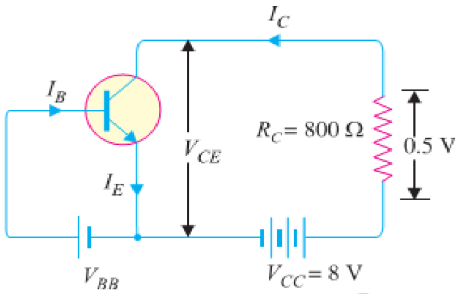
$\therefore$ $I_C = \frac{1\ V}{1\ K\Omega}$

Now $\beta = \frac{I_C}{I_B}$ $\therefore$ $I_B = \frac{I_C}{\beta} = \frac{1}{45} =$ **0.022 mA**

8. A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance R_C connected in the collector circuit is 0.5V. The value of R_C = 800 Ω. If α= 0.96, Determine :

(i) Collector-emitter voltage

(ii) Base current



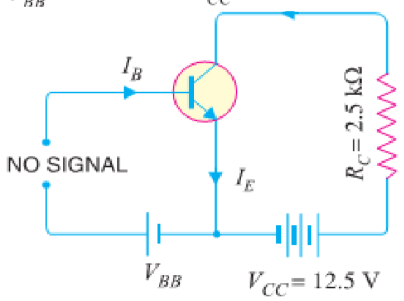
Solution: Fig. shows the required common emitter connection with Various values. (i) Collector-Emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \mathbf{7.5\ V}$$

(ii) The voltage drop across R_C (= 800 Ω) is 0.5 V.

$\therefore$ $I_C = \frac{0.5\ V}{800\ \Omega} = \frac{5}{8}$ mA = 0.625 mA

Now $\beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$ $\therefore$ Base current, $I_B = \frac{I_C}{\beta} = \frac{0.625}{24} =$ **0.026 mA**



9. For the circuit shown in Fig. , Draw the D.C. load line.

Solution: $V_{CE} = V_{CC} - I_C R_C$, When $I_C = 0$ ➔ $V_{CE} = V_{CC} =$ **12.5 V**

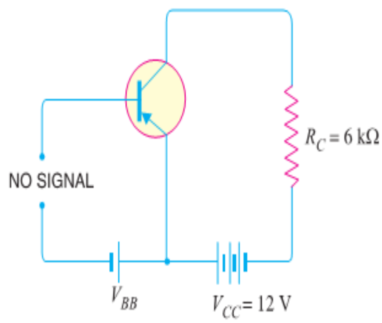
This locates the point B of the load line on collector – emitter voltage axis.

When $V_{CE} = 0$ ➔ $I_C = V_{CC} / R_C$ = 12.5V/2.5 kΩ = **5mA**

This locates the point A of the load line on collector current axis.

By joining these two points, we get the D.C. load line AB.

10. In the circuit diagram shown in Fig. (i), if V_{CC} = 12V and R_C = 6KΩ, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and β = 50?



Solution: The collector – emitter voltage V_{CE} is given by: $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} =$ **12V.** This locates the point B of the load line. When $V_{CE} = 0$, $I_C = V_{CC}/R_C$ = 12V/6 kΩ = **2 mA**. This locates the point A of Load Line. By joining these two points, load line AB is constructed.

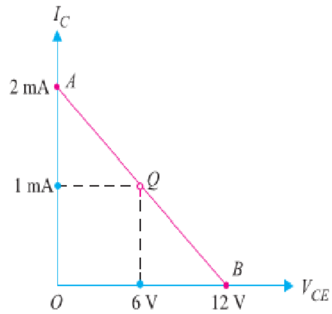
Zero signal base current, $I_B = 20\ \mu A = 0.02$ mA Current amplification factor, $\beta = 50$

∴ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 =$ **1 mA**

Zero signal collector – emitter voltage is $V_{CE} = V_{CC} - I_C R_C = 12 – 1mA \times 6\ k\Omega =$ **6V**.

∴ Operating point is 6V, 1mA

Fig. (ii) Shows the Q point. Its co-ordinate are I_C = 1mA and V_{CE} = 6V.

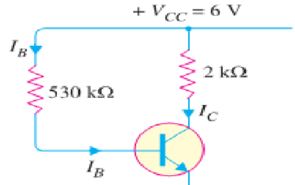


11. Fig. Shows that a silicon transistor with β = 100 is biased by Base resistor method. Draw D.C. the Load Line & Determine Operating point.

Solution: $V_{CC} = 6V$, $R_B = 530\ k\Omega$, $R_C = 2\ k\Omega$

D.C. Load Line. Referring to Fig. (i), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} =$ **6V**. This locates the first point B (OB = 6V) of load line on collector – emitter voltage axis as shown in Fig. (ii). When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 6V/2\ k\Omega =$ **3 mA.**



This locates the second point A (OA=3mA) of the load line on the collector current axis. By joining points A and B, D.C. Load Line AB is constructed.

Operating point Q. as it is silicon transistor, therefore, $V_{BE} = 0.7V$.

Referring to Fig. (i), it is clear that:

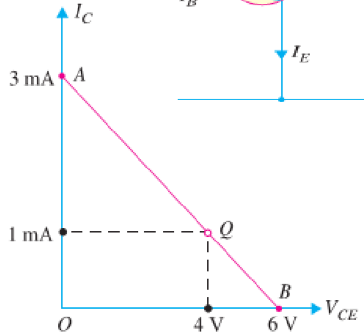
$$I_B R_B + V_{BE} = V_{CC}$$

Or $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6-0.7)\,V}{530\ k\Omega} = 10\mu A$$

∴ Collector current, $I_C = \beta\ I_B = 100 \times 10 = 1000\ \mu A =$ **1mA**

Collector-emitter voltage, $V_{CE} = V_{CC} – I_C R_C = 6 – 1mA \times 2\ k\Omega = 6 – 2 =$ **4V**

∴ Operating point is (4V, 1mA.) Fig. (ii) Shows the operating point Q on the D.C. load line. Its co-ordinates are I_C = 1mA and V_{CE} = 4V.



12. ***Fig. shows a silicon transistor biased by feedback resistor method. Determine the operating point. Given that β = 100.***

Solution: $V_{CC} = 20V$, $R_B = 100k\Omega$, $R_C = 1\ k\Omega$. Since it is silicon transistor, $V_{BE} = 0.7V$.

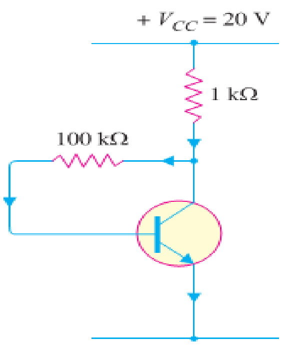
Assuming I_B to be in mA and using the relation,

$R_B = \frac{V_{CC} - V_{BE} - \beta\ I_B R_C}{I_B}$ Or $100 \times I_B = 20 – 0.7 – 100 \times I_B \times 1$ ➔ $200\ I_B = 19.3$

➔ $I_B = \frac{19.3}{200} = 0.096$ mA ∴ Collector current, $I_C = \beta\ I_B = 100 \times 0.096 =$ **9.6 mA**

Again $V_{CE} = V_{CC} – I_C R_C = 20 – 9.6\ mA \times 1\ k\Omega =$ **10.4 V**

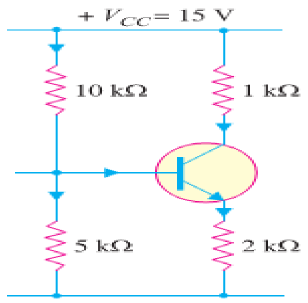
∴ Q-Point is (10.4V, 9.6mA.)



13. Fig. shows the voltage divider bias method. Draw the D.C. Load Line and determine the operating point. Assume the transistor to be of silicon.

Solution: *D.C. Load Line*. The collector-emitter voltage V_{CE} is given by:

$V_{CE} = V_{CC} – I_C (R_C + R_E)$ When $I_C = 0$, $V_{CE} = V_{CC} =$ **15V.**



♣ This locates the first point B (OB= 15V) of the load line on the collector-emitter voltage axis. When $V_{CE} = 0$, $I_C = V_{CC}/ (R_C + R_E) = 15\ V/ (1 + 2)\ k\Omega =$ **5 mA**

♣ This locates the second point A (OA=5mA) of the load line on collector current axis. By joining points A & B, the D.C. Load Line AB is constructed as in Fig.

Operating Point: - For silicon Transistor, $V_{BE} = 0.7$ V

Voltage across 5 kΩ is $V_2 = [V_{CC}/ (10+5)]*5$

Voltage drop across $R_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$

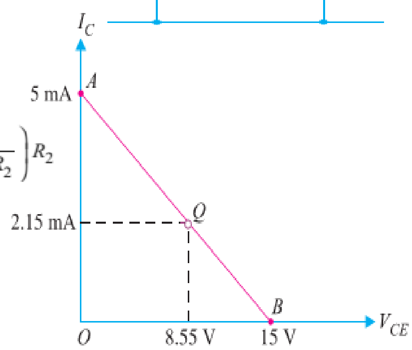
Or $V_2 = (15x5)/ (10+5) = 5$ V

∴ Emitter current, $I_E = (V_2 - V_{BE})/R_E = (5-0.7)/2k\Omega = 4.3/2k\Omega = 2.15$ mA

∴ Collector current is $I_C \approx I_E =$ **2.15 mA**

Collector-Emitter volt, $V_{CE} = V_{CC} – I_C (R_C + R_E) = 15 – 2.15mA \times 3k\Omega =$ **8.55V**

∴ Operating point is (8.55 V, 2.15 mA) is shown in Fig.

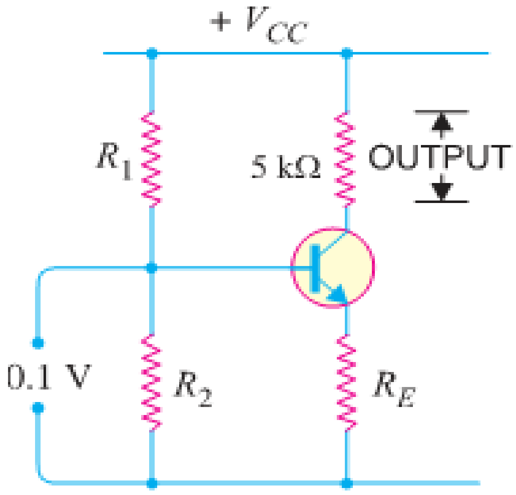


❖ AMPLIFIER:-

- The device which increases the strength of a weak signal is known as *Amplifier*. This can achieve by use of Transistor. It may be classified according to the number of stage of amplification, Such as:-
  1) Single stage transistor amplifier.
  2) Multi stage transistor amplifier.
- ✓ **Single Stage Transistor Amplifier: -** When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as *Single Stage Transistor Amplifier*.
- ✓ **Multi stage Transistor Amplifier:-**When a transistor circuit containing more than one stage of amplification is known as *Multi stage Transistor Amplifier*.

❖ SINGLE STAGE TRANSISTOR AMPLIFIER:-

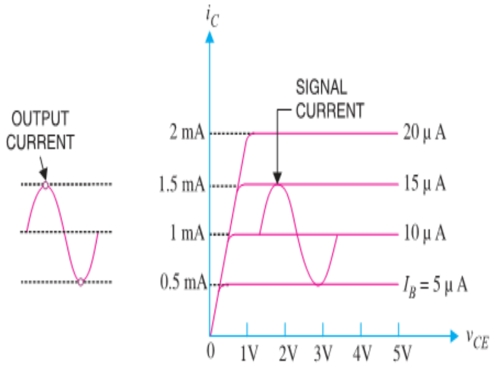
- A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components.
- When a weak A.C. signal is given to the base of transistor, a small base current starts flowing.
- Due to transistor action, a much larger (β times the base current) current flows through the collector load R_C.
- As the value of R_C is quite high (usually 4-10 kΩ), therefore, a large voltage appears across R_C.
- Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit.
- It is in this way that a transistor acts as an amplifier.



[Transistor as an Amplifier]

❖ Graphical Demonstration of Transistor Amplifier:-

- The function of transistor as an amplifier can also be explained graphically. The given Fig shows the output characteristics of a transistor in CE configuration.
- Suppose the zero signal base current is 10 μA i.e. this is the base current for which the transistor is biased by the biasing network.
- When an A.C. signal is applied to the base, it makes the base, say positive in the first half-cycle and negative in the second half cycle.
- Therefore, the base and collector currents will increase in the first half-cycle when base-emitter junction is more forward-biased.
- However, they will decrease in the second half-cycle when the base-emitter junction is less forward biased.



- For example, consider a sinusoidal signal which increases or decreases the base current by 5 μA in the two half-cycles of the signal. It is clear that in the absence of signal, the base current is 10μA and the collector current is 1 mA. However, when the signal is applied in the base circuit, the base current and hence collector current change continuously.
- In the first half-cycle peak of the signal, the base current increases to 15 μA and the corresponding collector current is 1.5 mA. In the second half-cycle peak, the base current is reduced to 5 μA and the corresponding collector current is 0.5 mA.
- For other values of the signal, the collector current is in between these values i.e. 1.5 mA and 0.5 mA. It is clear from above fig that 10 μA base current variation results in 1mA (1,000 μA) collector current variation i.e. by a factor of 100.
- This large change in collector current flows through collector resistance R_C. The result is that output signal is much larger than the input signal. Thus, the transistor has done amplification.

❖ MULTI STAGE TRANSISTOR AMPLIFIER:-

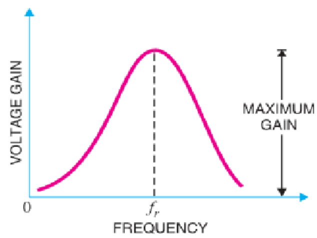
- The output from a single stage amplifier is usually insufficient to drive an output device. In other words, the gain of a single amplifier is inadequate for practical purposes.
- Consequently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is coupled in some way to the input of the next stage.
- The resulting system is referred to as multistage amplifier.

- A transistor circuit containing *more than one stage of amplification* is known as *multistage transistor amplifier*.
- In a multistage amplifier, a number of single amplifiers are connected in cascade arrangement i.e. output of first stage is connected to the input of the second stage through a suitable coupling device and so on.
- The purpose of **coupling device** (e.g. a capacitor, transformer etc.) is
  - (i) to transfer A.C. output of one stage to the input of the next stage and
  - (ii) to isolate the D.C. conditions of one stage from the next stage.
- The name of the amplifier is usually given after the type of coupling used. e.g.

Name of coupling	*Name of multistage amplifier*
RC coupling	R-C coupled amplifier
Transformer coupling	Transformer coupled amplifier
Direct coupling	Direct coupled amplifier

❖ IMPORTANT TERMS:-

- **Gain: -** The ratio of the output electrical quantity to the input one of the amplifier is called its gain.
- The gain of a multistage amplifier is equal to the product of gains of individual stages.
- For instance, if G_1, G_2 and G_3 are the individual voltage gains of a three-stage amplifier, then total voltage gain G is given by: $G = G_1 \times G_2 \times G_3$
- **Frequency response: -** The curve between voltage gain and signal frequency of an amplifier is known as frequency response.

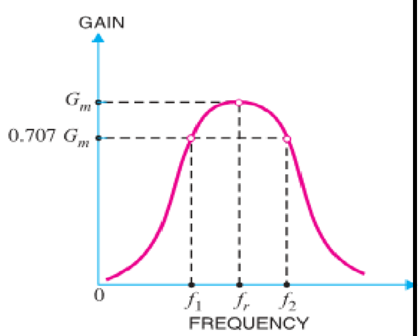


- The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at f_r, called resonant frequency.
- **Decibel gain: -** Although the gain of an amplifier can be expressed as a number, yet great practical importance to assign it a unit.
- The unit assigned is bel or decibel (db). The common logarithm (log to the base 10) of power gain is known as bel power gain i.e. $\text{Power gain} = \log_{10} \frac{P_{out}}{P_{in}}\ bel$ (1 bel=10 db.)
- Similarly voltage gain and current gain may be defined as follows:-

$$\text{Voltage gain in } db = 10 \log_{10} \frac{V_{out}^2 / R}{V_{in}^2 / R} = 20 \log_{10} \frac{V_{out}}{V_{in}}$$

$$\text{Current gain in } db = 10 \log_{10} \frac{I_{out}^2 R}{I_{in}^2 R} = 20 \log_{10} \frac{I_{out}}{I_{in}}$$

- **Bandwidth: -** The range of frequency over which the voltage gain is equal to or greater than 70.7% of the maximum gain is known as **bandwidth**.

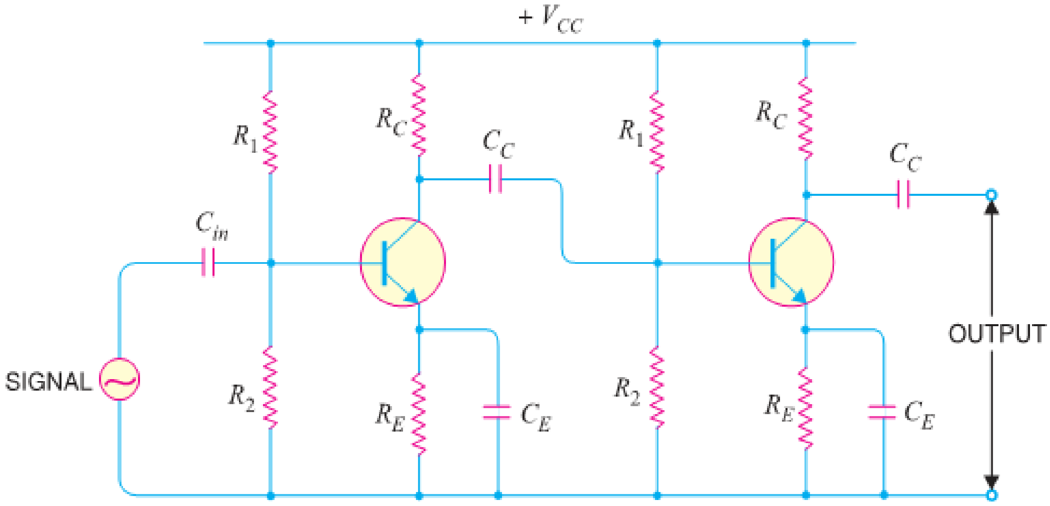


- From the fig. it is clear that for any frequency lying between f_1 and f_2, the gain is equal to or greater than 70.7% of the maximum gain.
- Therefore, $f_1 - f_2$ is the bandwidth. It may be seen that f_1 and f_2 are the limiting frequencies. The f_1 is called lower cut-off frequency and f_2 is known as upper cut-off frequency

❖ R-C COUPLED TRANSISTOR AMPLIFIER:-

- This is the most popular type of coupling because it is cheap and *provides excellent audio fidelity over a wide range of frequency*. It is usually employed for **voltage amplification**.
- Fig shows two stages of an RC coupled amplifier. A coupling capacitor C_C is used to connect the output of first stage to the base (i.e. input) of the second stage and so on.
- As the coupling from one stage to next is achieved by a coupling capacitor followed by a connection to a shunt resistor, therefore, such amplifiers are called ***Resistance - Capacitance coupled amplifiers***.

- The resistances R_1, R_2 and R_E form the *biasing* and *stabilization* network. The emitter bypass capacitor offers *low reactance path* to the signal. Without it, the voltage gain of each stage would be lost.
- The coupling capacitor C_C transmits A.C. signal but blocks D.C. This prevents D.C. interference between various stages and the shifting of operating point.



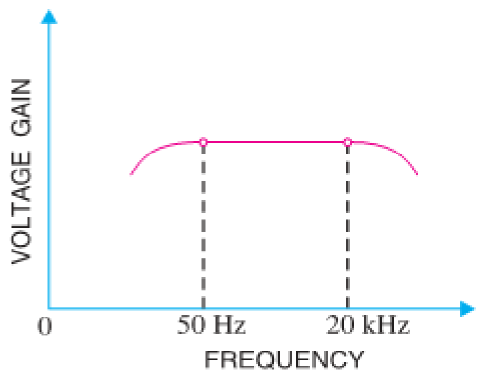
[Circuit Diagram of RC Coupled Transistor Amplifier]

- **Operation: -** When A.C. signal is applied to the base of the first transistor, it appears in the amplified form across its collector load R_C. The amplified signal developed across RC is given to base of next stage through coupling capacitor C_C. The second stage does further amplification of the signal. In this way, the cascaded (one after another) stages amplify the signal and the overall gain is considerably increased.

It may be mentioned here that total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the effective load resistance of first stage is reduced due to the shunting effect of the input resistance of second stage. This reduces the gain of the stage which is loaded by the next stage

FREQUENCY RESPONSE:

- Fig shows the frequency response of a typical RC coupled amplifier. It is clear that voltage gain drops off at low (< 50 Hz) and high (> 20 kHz) frequencies whereas it is uniform over mid-frequency range (50 Hz to 20 kHz). This behaviour of the amplifier is briefly explained below:-
- **(i) At low frequencies** (< 50 Hz):- At this stage the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass from one stage to the next stage. Moreover, C_E cannot shunt the emitter resistance R_E effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.
- **(ii) At high frequencies** (> 20 kHz):-At this stage the reactance of C_C is very small and it behaves as a short circuit. These increases the loading effect of next stage and serves to reduce the voltage gain.
Moreover, at high frequency, capacitive reactance of base-emitter junction is low which increases the base current. This reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.



[Frequency Response Curve of RC Coupled Amp]

- **(iii) At mid-frequencies** (50 Hz to 20 kHz):- At this stage the voltage gain of the amplifier is constant. The effect of coupling capacitor in this frequency range is such so as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of CC decreases which tends to increase the gain. However, at the same time, lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.

Advantages:-

(i) It has excellent frequency response. The gain is constant over the audio frequency range which is the region of most importance for speech, music etc.
(ii) It has lower cost since it employs resistors and capacitors which are cheap.
(iii) The circuit is very compact as the modern resistors and capacitors are small and extremely light.

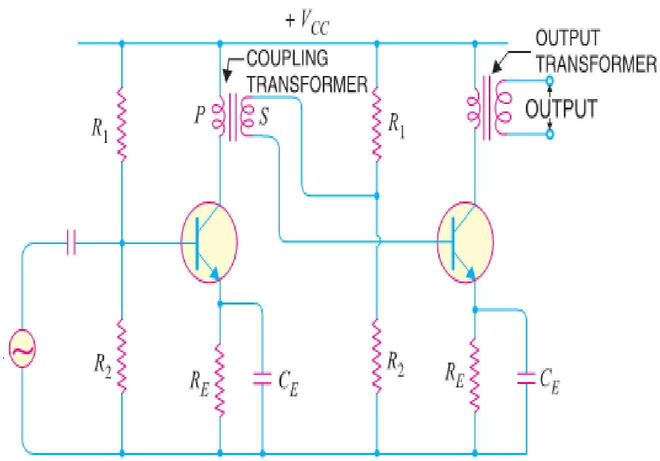
Disadvantages:-

(i) The RC coupled amplifiers have low voltage and power gain. It is because the low resistance presented by the input of each stage to the preceding stage decreases the effective load resistance (R_{AC}) and hence the gain.
(ii) They have the tendency to become noisy with age, particularly in moist climates.
(iii) Impedance matching is poor. It is because the output impedance of RC coupled amplifier is several hundred ohms whereas the input impedance of a speaker is only a few ohms. Hence, little power will be transferred to the speaker.

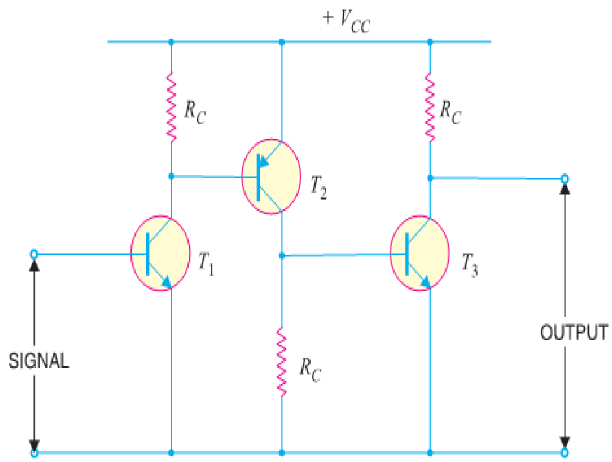
Applications:-

- The RC coupled amplifiers have excellent audio fidelity over a wide range of frequency. Therefore, they are widely used as **voltage amplifiers** e.g. in the initial stages of public address system.
- If other type of coupling (e.g. transformer coupling) is employed in the initial stages, this results in frequency distortion which may be amplified in next stages.
- However, because of poor impedance matching, RC coupling is rarely used in the final stages.

✓ **Circuit diagram for Other Type of Coupling are given below:-**



(Transformer Coupled Transistor Amplifier)

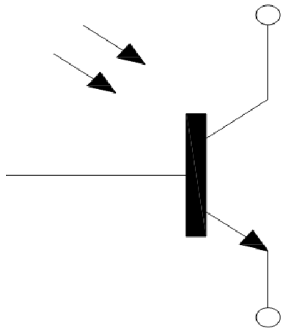


(Direct Coupled Transistor Amplifier)

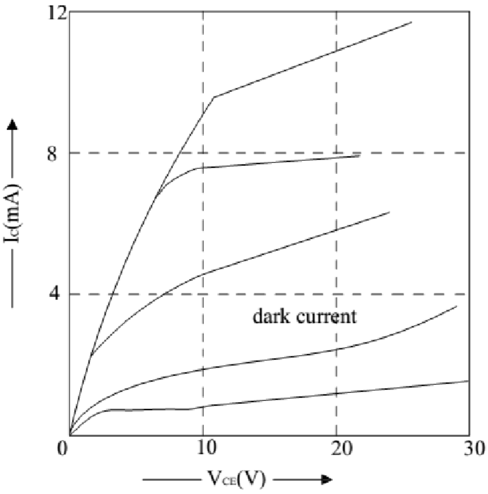
➢ **Comparison of Different Types of Coupling:-**

S. No	Particular	*RC* coupling	Transformer coupling	Direct coupling
1.	*Frequency response*	Excellent in the audio frequency range	Poor	Best
2.	*Cost*	Less	More	Least
3.	*Space and weight*	Less	More	Least
4.	*Impedance matching*	Not good	Excellent	Good
5.	*Use*	For voltage amplification	For power amplification	For amplifiying extremely low frequencies

❖ PHOTO TRANSISTOR: -

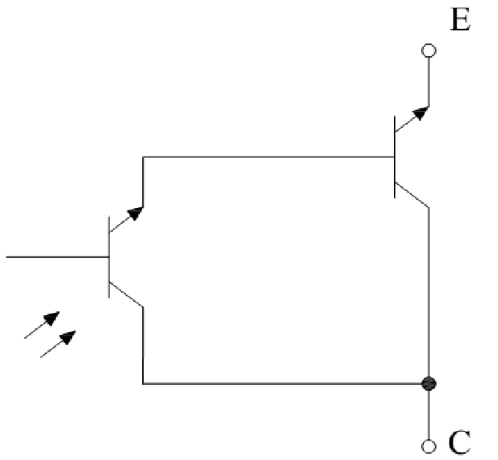


- It is light sensitive Transistor and is similar to an ordinary BJT except that it has no connection to the base terminal. Its operation is based on the photo diode that exits at CB junction.
- Instead of the base current, the input to the transistor is provided in the form of light as shown in symbol.
- Silicon NPNs are mostly used as photo Transistor. The device is usually is packed in a TO-type can with a lens on top although it is sometimes encapsulated in clear plastic.
- When there is no incident light on the CB junction, there is a small thermally generated collector-to-emitter leakage current I_{CEO} which, in this case is called **dark current** and is in the nA range.
- When light is incident on the CB junction, a base current I_λ is produced which is directly proportional to the light intensity. Hence, collector current $I_C=\beta I_\lambda$.
- Typical collector characteristic curve of a photo transistor are shown in fig. each individual curves corresponds to a certain value of light intensity expressed in mW/cm^2. As seen I_C increases with light intensity.
- The phototransistor has applications similar to those of a photo diode. Their main differences are in the current and response time. The photo transistor has the advantages of greater sensitivity and current capacity than photo diodes.
- However, photo diodes are faster of the two, switching in less than a nanosecond.



❖ PHOTO DARLINGTON: -

- As shown in fig. a Photo Darlington consists of a photo transistor in a Darlington arrangement with a common transistor.
- It has a much greater sensitivity to incident radiant energy than a photo transistor because of higher current gain.
- However, its switching time of 50μs is much longer than the photo transistor (2μs) or the photo diode (1ns). Its circuit symbol is shown in fig.
- Photo Darlington is used in a variety of application some of which are given below.
- A *light operated relay* in which the photo transistor Q_1 drives the bipolar transistor Q_2. When sufficient light falls on Q_1 it is driven into saturation so that I_C is increased multiple. This collector current while passing through the relay coil energizes the relay.



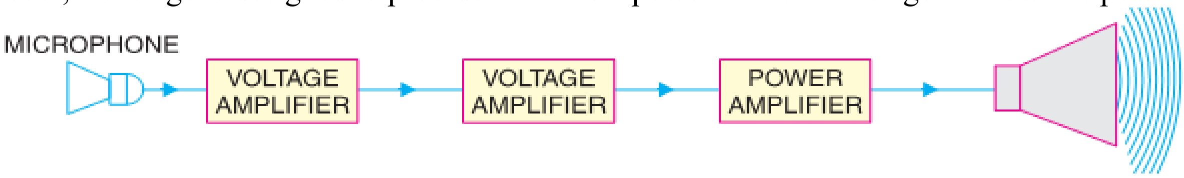
- A *dark operated relay* circuit i.e. one in which relay is deenergized when light falls on the photo transistor.
- Such relays are used in many applications such as
  (i) Automatic door activators
  (ii) Process Counters
  (iii) Various alarm systems for smoke or interference detection.

[CHAPTER-3]

[AUDIO POWER AMPLIFIERS]

❖ INTRODUCTION:-

- A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device.
- The first few stages in this multistage amplifier have the function of only voltage amplification. However, last stage is designed to provide maximum power. This final stage is known as power stage.



❖ Transistor Audio Power Amplifier: -

- A transistor amplifier which raises the power level of the signals having audio frequency range is known as transistor **Audio Power Amplifier**. Generally last stage of a multistage amplifier is the power stage.
- The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power.
- A transistor that is suitable for power amplification is generally called a *power transistor*.

❖ DIFFERENCE BETWEEN VOLTAGE AND POWER AMPLIFIERS

- The difference between the two types is really one of degree; it is a question of how much voltage and how much power.
- A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level.
- On the other hand, a power amplifier is designed to obtain maximum output power.

1) **Voltage Amplifier.** The voltage gain of an amplifier is given by : $\mathbf{A_v = \beta \times \frac{R_c}{R_{in}}}$

- In order to achieve high voltage amplification, the following features are incorporated in such amplifiers:
  - ♣ The transistor with high β(>100) is used in the circuit. i.e. Transistors are employed having thin base.
  - ♣ The input resistance R_{in} of transistor is sought to be quite low as compared to the collector load R_C.
  - ♣ A relatively high load R_C is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (≈ mA). If the collector current is small, we can use large R_C in the collector circuit

2) **Power Amplifier.** A power amplifier is required to deliver a large amount of power and as such it has to handle large current.

- In order to achieve high power amplification, the following features are incorporated in such amplifiers :
  - ♣ The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.
  - ♣ The base is made thicker to handle large currents. In other words, transistors with comparatively smaller β are used.
  - ♣ Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form :

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually $R - C$ coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

❖ PERFORMANCE QUANTITIES OF POWER AMPLIFIERS

- The prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are : **Collector Efficiency, Distortion & Power Dissipation Capability**

Collector efficiency.

- The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output.
- Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as *collector efficiency* and may be defined as under :
  - ♣ The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as **collector efficiency**.

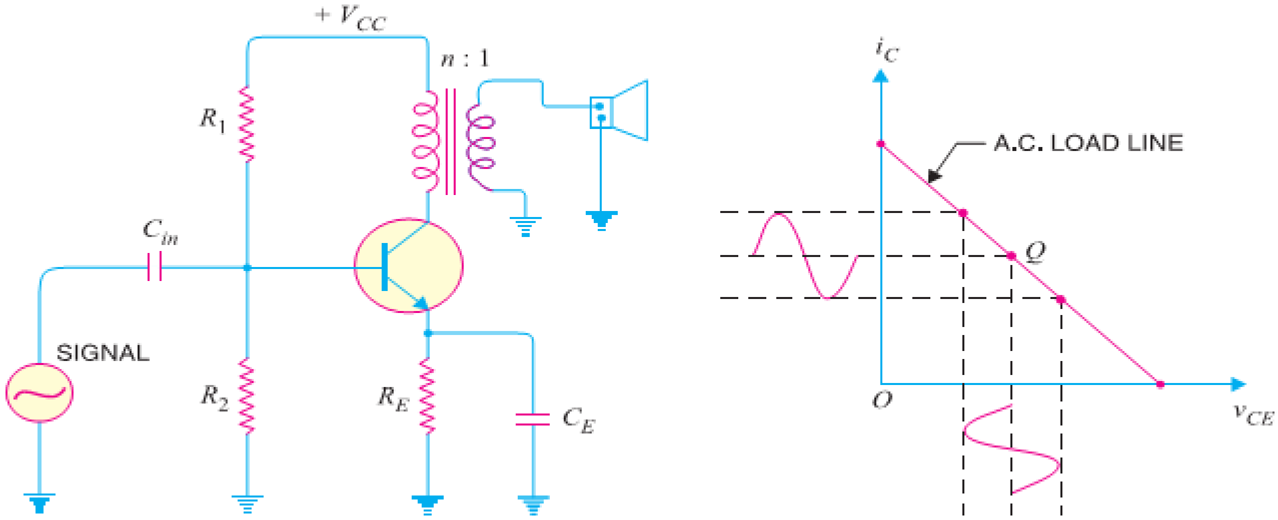
Distortion. The change of output wave shape from input wave shape of amplifier is called **Distortion**.

Power Dissipation Capability. The ability of a power transistor to dissipate heat is known as power dissipation capability.

❖ CLASSIFICATION OF POWER AMPLIFIERS

- Transistor power amplifiers handle large signals. Many of them are driven by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle.
- Therefore, such amplifiers are generally classified according to their mode of operation i.e. the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as
  (i) Class A power amplifier **(ii)** Class B power amplifier **(iii)** Class C power amplifier

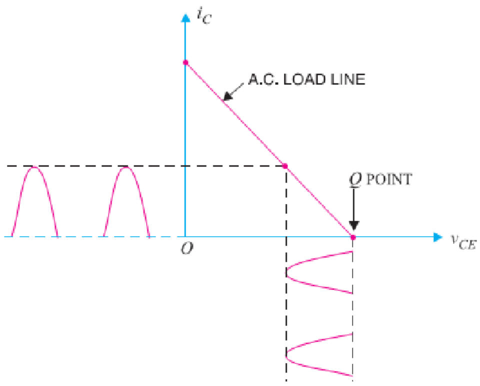
CLASS A POWER AMPLIFIER. If the collector current flows at all times during the full cycle of the signal, the power amplifier is known as *class A power amplifier*.



- The power amplifier must be biased in such a way that no part of the signal is cut off. Fig (i) shows circuit of class A power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers.
- The use of transformer permits impedance matching, resulting in the transference of maximum power to the load e.g. loudspeaker. Fig (ii) shows the class A operation in terms of a.c. load line.
- The operating point Q is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion.
- However, they have the disadvantage of low power output and low collector efficiency (about 35%).

CLASS B POWER AMPLIFIER: - If the collector current flows only during the positive half-cycle of the input signal, it is called a *class B power amplifier*.

- In class B operation, the transistor bias is so adjusted that zero signal collector current is zero i.e. no biasing circuit is needed at all.
- During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows.



- Fig. shows the class B operation in terms of a.c. load line.
- The operating point Q shall be located at collector cut off voltage.
- It is easy to see that output from a class B amplifier is amplified half-wave rectification.
- In a class B amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs.
- However, class B amplifiers provide higher power output and collector efficiency (50 − 60%).
- Such amplifiers are mostly used for power amplification in push-pull arrangement.
- In such an arrangement, 2 transistors are used in class B operation. One transistor amplifies the positive half cycle of the signal while the other amplifies the negative half-cycle.

CLASS C POWER AMPLIFIER. If the collector current flows for less than half-cycle of the input signal, it is called *class C power amplifier*.

- In class C amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts.
- Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers i.e. to amplify a narrow band of requencies near the resonant frequency.

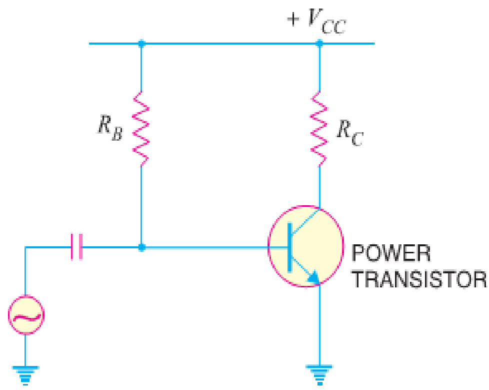
EXPRESSION FOR COLLECTOR EFFICIENCY

- For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.
- Now, Collector Efficiency, $\eta = \dfrac{\text{a.c. power output}}{\text{d.c. power input}} = \dfrac{P_O}{P_{dc}}$
- Where $P_{dc} = V_{CC}\, I_C$ & $P_O = V_{CE}\, I_C$ in which V_{CE} is the r.m.s. value of signal output voltage and I_c is the r.m.s. value of output signal current.
- In terms of peak-to-peak values, the a.c. power output can be expressed as:

$P_o = [(0.5\times0.707)\, v_{ce(p-p)}][(0.5\times0.707)\, i_{c(p-p)}] = \dfrac{V_{ce(p-p)} \times i_{c(p-p)}}{8}$ [As,0.5×0.707×0.5×0.707=0.125=**1/8**]

$$\therefore \qquad \textbf{Collector } \boldsymbol{\eta} = \frac{V_{ce(p-p)} \times i_{c(p-p)}}{8\, V_{cc}\, I_c}$$

MAXIMUM COLLECTOR EFFICIENCY OF SERIES-FED CLASS A AMPLIFIER : -



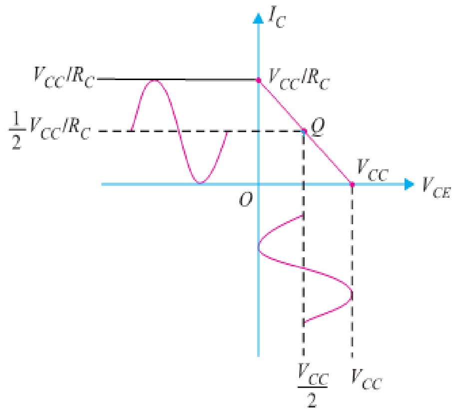
- Fig (i) shows a series fed class A amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency.
- Nevertheless, it will help the reader to understand the class A operation. The d.c. load line of the circuit is shown in Fig. (ii).
- When an ac signal is applied to the amplifier, the output current and voltage will vary about the operating point Q.
- In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the Q point should be located at the centre of the dc load line.
- In that case, operating point is $I_C = V_{CC}/2R_C$ and $V_{CE} = V_{CC}/2$.

Maximum $v_{ce(p-p)} = V_{CC}$ Maximum $i_{c(p-p)} = V_{CC}/R_C$

Max. a.c. output power, $P_{o(max)} = \dfrac{V_{ce(p-p)} \times i_{c(p-p)}}{8} = \dfrac{V_{CC} \times V_{CC}/R_C}{8} = \dfrac{V_{CC}^2}{8R_C}$

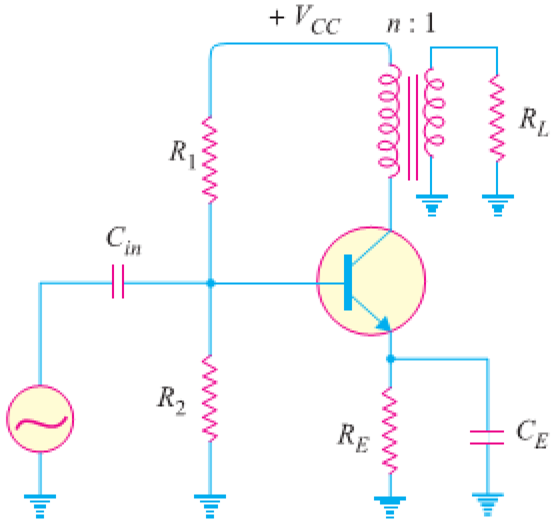
D.C. power supplied, $P_{dc} = V_{CC}\, I_C = V_{CC}\left(\dfrac{V_{CC}}{2R_C}\right) = \dfrac{V_{CC}^2}{2R_C}$

$$\therefore \qquad \text{Maximum collector } \eta = \frac{P_{O\,(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = \mathbf{25\%}$$

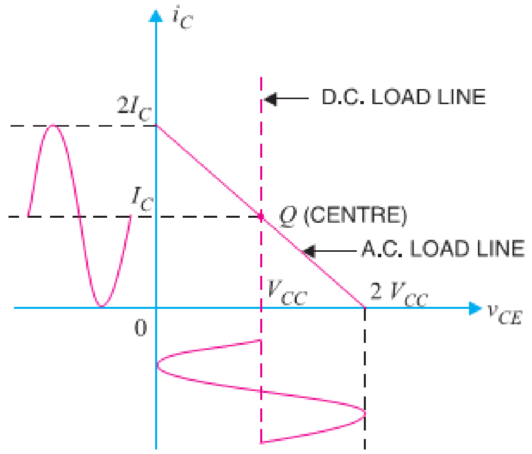


- Thus the maximum collector efficiency of a class A series-fed amplifier is 25%.
- In actual practice, collector efficiency is far less than this value.

Maximum Collector Efficiency Of Transformer Coupled Class A Power Amplifier : -



- In class A power amplifier, the load can be either connected directly in the collector or it can be transformer coupled.
- But Transformer coupled method is often preferred for two main reasons. **First,** transformer coupling permits impedance matching. **Secondly** it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.
- Fig(i) shows a transformer coupled class A power amplifier.
- In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig (ii).
- Under zero signal conditions, the effective resistance in the collector circuit is that of primary winding of Transformer.
- The primary resistance has a very small value and is assumed zero. Therefore, d.c. load line is a vertical line rising from V_{CC} as shown in Fig. (ii).



- When signal is applied, the collector current will vary about the operating point Q.
- In order to get maximum a.c. power output (Hence maximum collector η), the peak value of collector current due to signal alone should be equal to the zero signal collector current I_C.
- In terms of a.c. load line, the operating point Q should be located at the centre of a.c. load line.
- During the peak of the positive half-cycle of the signal, the total collector current is 2 I_C and $v_{ce} = 0$. During the negative peak of the signal, the collector current is zero and $v_{ce} = 2V_{CC}$.

  ∴ Peak-to-peak collector-emitter voltage is

  $$v_{ce(p-p)} = 2V_{CC}$$

  Peak-to-peak collector current, $i_{c(p-p)} = 2\ I_C = \frac{V_{ce(p-p)}}{R'_L} = \frac{2V_{CC}}{R'_L}$

  Where R'_L is the reflected value of load R_L and appears in primary of the transformer.
- If n ($= N_p/N_s$) is the turn ratio of the transformer, then, $R'_L = n^2 R_L$.
- d.c. power input, $P_{dc} = V_{CC}\ I_C = I_C^2 R'_L$ (∵ $V_{CC} = I_C\ R'_L$)
- Max. a.c. output power, $P_{o(max)} = \frac{V_{ce(p-p)} \times i_{c(p-p)}}{8} = \frac{2V_{CC} \times 2I_C}{8} = \frac{1}{2} V_{CC}\ I_C = \frac{1}{2} I_C^2 R'_L \ldots$ (i) (∵ $V_{CC} = I_C\ R'_L$)

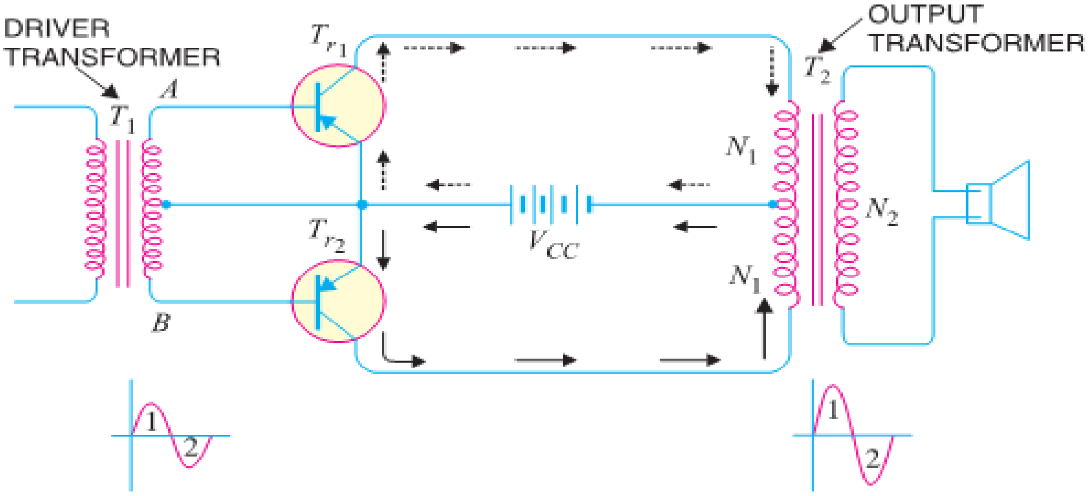
  ∴ Max. Collector $\eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{\left(\frac{1}{2}\right) I_C^2 R'_L}{I_C^2 R'_L} \times 100 =$ **50%**

IMPORTANT POINTS ABOUT CLASS-A POWER AMPLIFIER : -

- **(i)** A Transformer coupled class A power amplifier has a maximum collector efficiency of 50% i.e., maximum of 50% d.c. supply power is converted into a.c. power output.
- In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.
- **(ii)** The power dissipated by a transistor is given by : $P_{dis} = P_{dc} - P_{ac}$

  Where Pdc= available d.c. power & P_{ac} = available a.c. power
- So, In class A operation, Transistor must dissipate less heat when signal is applied therefore runs cooler.
- **(iii)** When no signal is applied to a class A power amplifier, $P_{ac} = 0$. ∴ P_{dis} = Pdc
- Thus in class A operation, maximum power dissipation in the transistor occurs under zero signal conditions.
- Therefore, the power dissipation capability of a power transistor (for class A operation) must be at least equal to the zero signal rating.
- **(iv)** When a class A power amplifier used in final stage, it is called single ended class A power amplifier.

PUSH-PULL AMPLIFIER : -



- The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. shows the circuit of a push-pull amplifier.
- Two transistors T_{r1} and T_{r2} placed back to back are employed. Both transistors are operated in class B operation i.e. collector current is nearly zero in the absence of the signal.
- The centre tapped secondary of driver transformer T_1 supplies equal and opposite voltages to the base circuits of two transistors. The output transformer T_2 has the centre-tapped primary winding. The supply voltage V_{CC} is connected between the bases and this centre tap.
- The loudspeaker is connected across the secondary of this transformer.

CIRCUIT OPERATION.

- The input signal appears across the secondary AB of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end A becomes positive and end B negative.
- This will make the base-emitter junction of T_{r1} reverse biased and that of T_{r2} forward biased. The circuit will conduct current due to T_{r2} only and is shown by solid arrows.
- Therefore, this half-cycle of the signal is amplified by T_{r2} and appears in the lower half of the primary of output transformer. In the next half cycle of the signal, T_{r1} is forward biased whereas T_{r2} is reverse biased. Therefore, T_{r1} conducts and is shown by dotted arrows.
- Consequently, this half-cycle of the signal is amplified by T_{r1} and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.
- It may be noted here that push-pull arrangement also permits a maximum transfer of power to the Load through impedance matching. If R_L is the resistance appearing across secondary of output transformer, then resistance R'_L of primary shall become:

$$\mathbf{R'_L = \left(\frac{2N_1}{N_2}\right)^2 R_L}$$

Where N_1 = Number of turns between either end of primary winding and centre-tap
N_2 = Number of secondary turns

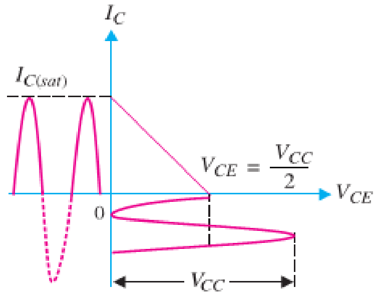
ADVANTAGES

1) The efficiency of the circuit is quite high (≈75%) due to class B operation.
2) A high a.c. output power is obtained.

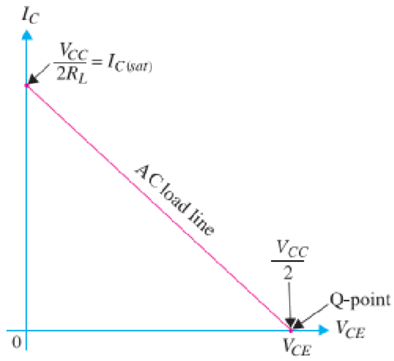
DISADVANTAGES

1) Two transistors have to be used.
2) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.
3) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.
4) The circuit gives more distortion.
5) Transformers used are bulky and expensive.

MAXIMUM EFFICIENCY FOR CLASS B POWER AMPLIFIER



- We have already seen that a push-pull circuit uses two transistors working in class B operation. For class B operation, the Q-point is located at cut-off on both d.c. and a.c. load lines.
- For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. (i). It is clear that a.c. output voltage has a peak value of V_{CE} and a.c. output current has a peak value of $I_{C(sat)}$.
- The same information is also conveyed through the a.c. load line for the circuit [See Fig. (ii)].



∴ Peak a.c. output voltage = V_{CE}

Peak a.c. output current = $I_{C(sat)} = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{2R_L}$ $\left(\because V_{CE} = \frac{V_{CC}}{2}\right)$

- Maximum average a.c. output power $P_{o\,(max)}$ is the Product of r.m.s. values of a.c. output voltage and a.c. output current

$$= \frac{V_{CE}}{\sqrt{2}} \times \frac{I_{C(sat)}}{\sqrt{2}} = \frac{V_{CE} I_{C(sat)}}{2} = \frac{V_{CC}}{2} \times \frac{I_{C(sat)}}{2} = \frac{V_{CC} I_{C(sat)}}{4} \quad \left(\because V_{CE} = \frac{V_{CC}}{2}\right)$$

∴ $\mathbf{P_{o(max)} = 0.25\, V_{CC} I_{C(sat)}}$

- The input d.c. power from the supply V_{CC} is $\mathbf{P_{dc} = V_{CC}\, I_{dc}}$
  Where I_{dc} is the average current drawn from the supply V_{CC}.
- Since the transistor is on for alternating half cycles, it effectively acts as a half-wave rectifier.

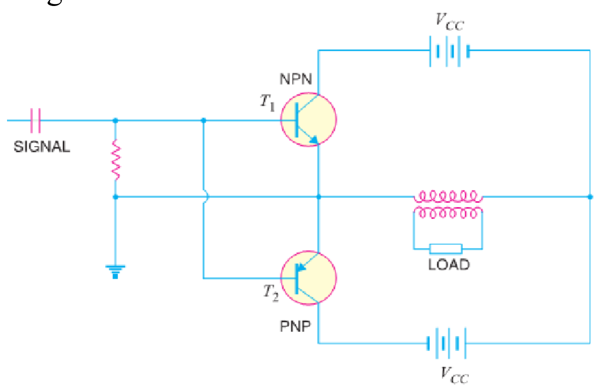
∴ $I_{dc} = \frac{I_{C(sat)}}{\pi}$ ➔ $P_{dc} = \frac{V_{CE} I_{C(sat)}}{\pi}$

∴ Max. Collector $\eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{0.25 V_{CC} I_{C(sat)}}{(V_{CC} I_{C(sat)})/\pi} \times 100 = 0.25\pi \times 100 = \mathbf{78.5\ \%}$

- Thus the maximum collector efficiency of class B power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

COMPLEMENTARY-SYMMETRY AMPLIFIER

- By complementary symmetry is meant a principle of assembling push-pull class B amplifier without requiring centre-tapped transformers at the input and output stages.
- Fig. shows the transistor push-pull amplifier using complementary symmetry. It employs one npn and one pnp transistor and requires no centre-tapped transformers.



- The circuit action is as follows. During the positive-half of the input signal, transistor T_1 (the npn transistor) conducts current while T_2(the pnp transistor) is cutoff.
- During the negative half-cycle of the signal, T_2 conducts while T_1 is cut off. In this way, npn transistor amplifies the positive half-cycles of the signal while the pnp transistor amplifies the negative half-cycles of the signal.
- Note that we generally use an output transformer (not centre-tapped) for impedance matching.

Advantages: - (1) This circuit does not require transformer. This saves on weight and cost.
(2) Equal and opposite input signal voltages are not required.

Disadvantages:- (1) It is difficult to get a pair of transistors (npn & pnp) having similar characteristics.
(2) We require both positive and negative supply voltages.

HEAT SINK: -

- As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat must be dissipated to the surroundings to keep the temperature within allowed limits.
- Usually transistor is fixed on Aluminum metal sheet so that additional heat is transferred to the Al sheet.
- The metal sheet that serves to dissipate the additional heat from power transistor is known as **Heat Sink.**

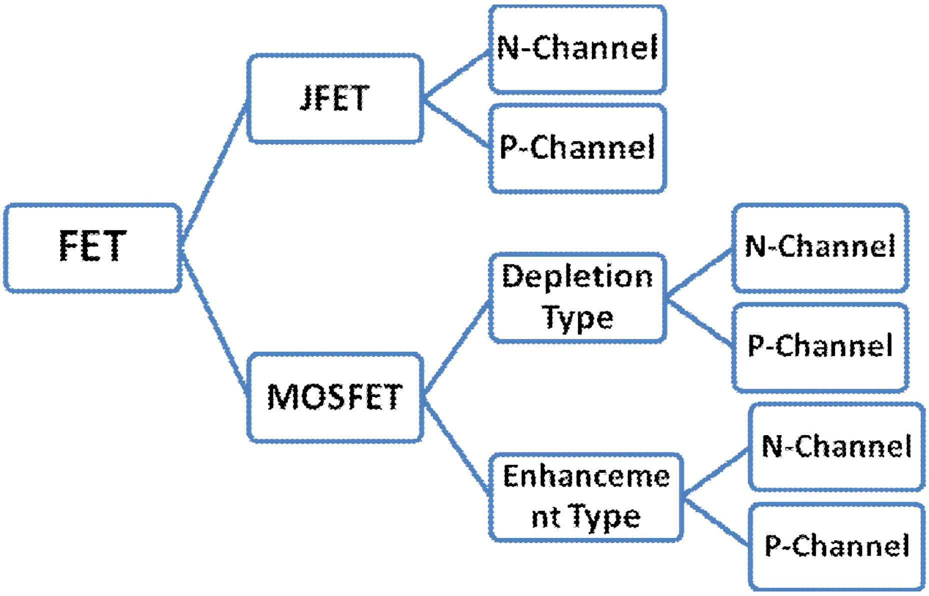
[CHAPTER-4]

------------------------- [FIELD EFFECT TRANSISTOR (FET)] -------------------------

❖ INTRODUCTION: -

- In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a **Bipolar Transistor.**
- The ordinary or bipolar transistor has two principal disadvantages. **First**, it has low input impedance because of forward biased emitter junction. **Secondly**, it has considerable noise level.
- Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few mega ohms.
- The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 mega ohms.
- The FET is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding FET market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications.

❖ CLASSIFICATION OF FIELD EFFECT TRANSISTORS: -



❖ Other types of C-MOS also There Such as: -**CMOS, VMOS, LDMOS** etc.

❖ DIFFERENTIATION BETWEEN BJT & FET : -

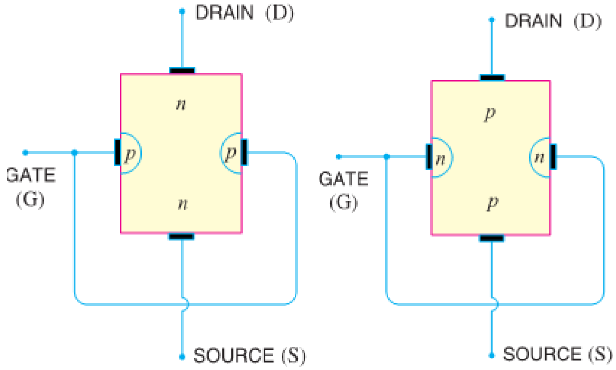
FET	BJT
✖ It means **Field Effect Transistor**	✖ Means **Bipolar Junction Transistor**
✖ Its three terminals are **Source, Gate & Drain**	✖ Its terminals are **Emitter, Base & Collector.**
✖ It is **Unipolar** devices i.e. Current in the device is carried either by electrons or holes.	✖ It is **Bipolar** devices i.e. Current in the device is carried by both electrons and holes.
✖ It is **Voltage controlled device.** i.e. Voltage at the gate or drain terminal controls the amount of current flowing through the devices.	✖ It is **Current controlled device.** i.e. Base Current controls the amount of collector current flowing through the devices.
✖ It has very High Input Resistance and Low Output Resistance.	✖ It has very Low Input Resistance and High Output Resistance.
✖ Low noisy operation	✖ High noisy operation
✖ It is Longer Life & High Efficiency.	✖ It is Shorter Life & Low Efficiency.
✖ It is much simpler to fabricate as IC and occupies less space on IC.	✖ It is comparatively difficult to fabricate as IC and occupies more space on IC then FET.
✖ It has Small gain bandwidth product.	✖ It has Large gain bandwidth product.
✖ It has higher switching speed.	✖ It has higher switching speed.

❖ JUNCTION FIELD EFFECT TRANSISTOR (JFET) : -

- A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.
- In a JFET, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device.
- The JFET has high input impedance and low noise level.

❖ CONSTRUCTIONAL DETAILS.

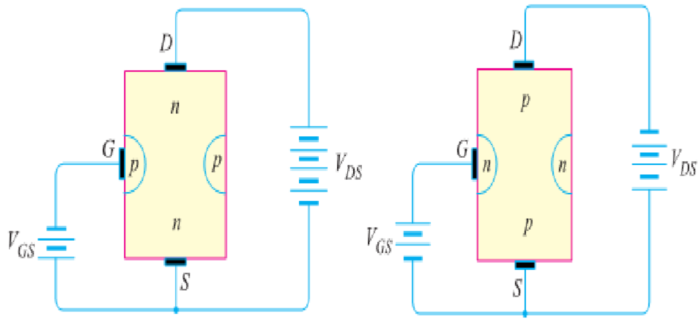
- A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in Fig.
- The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called n-channel JFET as shown in Fig (i) and if the bar is of p-type, it is called a p-channel JFET as shown in Fig (ii).
- The two pn junctions forming diodes are connected internally & a common terminal called **gate** is taken out.
- Other terminals are **source** and **drain** taken out from the bar as shown. Thus a JFET has essentially three terminals viz., Gate (G), Source (S) & Drain (D).



n-Channel JFET *p-Channel JFET*

❖ JFET POLARITIES: -

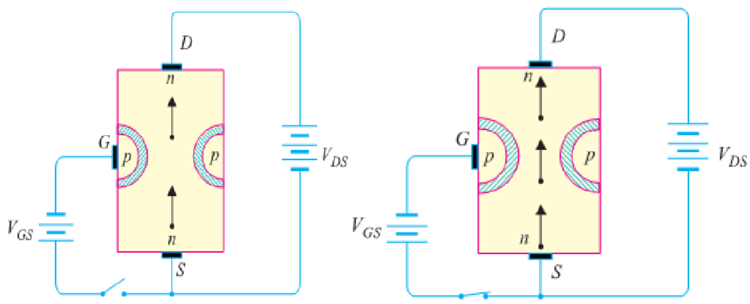
- Fig (i) shows n-channel JFET polarities whereas Fig (ii) shows the p-channel JFET polarities.
- Note that in each case, voltage between gate and source is such that the gate is reversing biased.
- This is the normal way of JFET connection.
- The drain & source terminals are interchangeable i.e., either end can be used as source and the other end as drain.



- The following points may be noted:
  - ♣ The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.
  - ♣ The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.
  - ♣ In all JFETs, source current I_S is equal to the drain current i.e. $I_S = I_D$.

❖ WORKING PRINCIPLE OF JFET:-

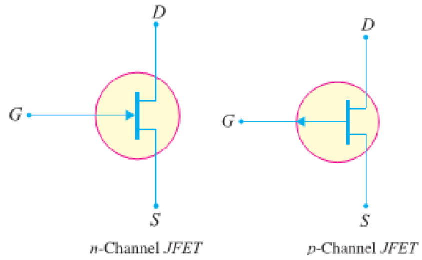
- **Principle: -** Fig. shows the circuit of n-channel JFET with normal polarities. Note that the gate is reverse biased.
- The two pn junctions at the sides form two depletion layers. The current conduction by charge carriers (i.e. free electrons in this case) is through the channel between the two depletion layers and out of the drain.



- The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}.
- The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease.
- Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.
- In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.
- **Working: -** The working of JFET is as under :
- **(i)** When voltage V_{DS} is applied between drain & source terminals and voltage on the gate is zero [See the above Fig (i)], the two pn junctions at the sides of the bar establish depletion layers.
- The electrons will flow from source to drain through a channel between the depletion layers.

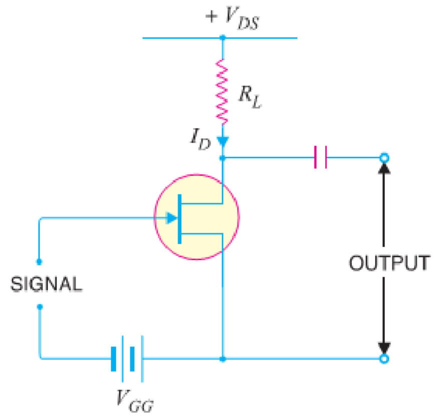
- The size of these layers determines width of the channel & hence the current conduction through the bar.
- **(ii)** When a reverse voltage V_{GS} is applied between the gate and source [See Fig (ii)], the width of the depletion layers is increased.
- This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased.
- On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.
- It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate.
- For this reason, the device is called field effect transistor. It may be noted that a p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

JFET AS AN AMPLIFIER :-



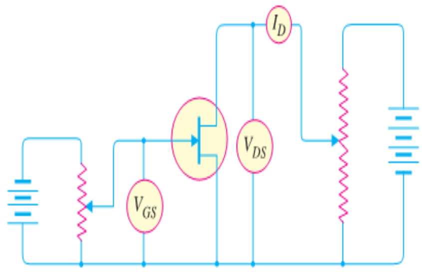
[Schematic Symbol of JFET]

- Fig shows JFET amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of JFET, the gate must be negative w.r.t. source i.e., input circuit should always be reverse biased.
- This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit.
- In the present case, we are providing biasing by the battery V_{GG}. A small change in the reverse bias on the gate produces a large change in drain current.



- This fact makes JFET capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current.
- During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases.
- The result is that a small change in voltage at the gate produces a large change in drain current.
- These large variations in drain current produce large output across the load R_L. In this way, JFET acts as an amplifier

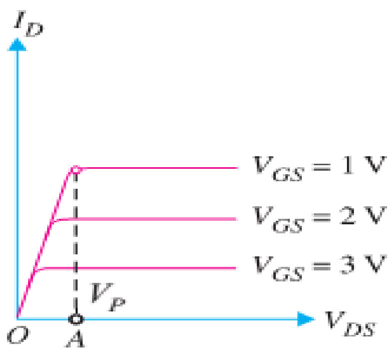
OUTPUT CHARACTERISTICS OF JFET



- The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET at constant gate source voltage (V_{GS}) is known as output characteristics of JFET.
- Fig shows circuit for determining output characteristics of JFET.
- Keeping V_{GS} fixed at some value, say 1V, the drain source voltage is changed in steps.
- Corresponding to each value of V_{DS}, the drain current I_D is noted.
- A plot of these values gives output characteristic of JFET at V_{GS}= 1V.
- Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. shows a family of output characteristics.

The following points may be noted from the characteristics:

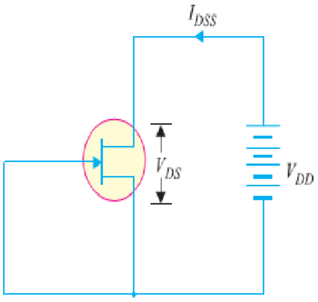
- **(i)** At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant.
- The drain-source voltage above which drain current becomes constant is known as pinch off voltage. Thus in Fig. OA is the pinch off voltage V_P.
- **(ii)** After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other.
- The drain current passes through the small passage between these layers.
- Thus increase in drain current is very small with V_{DS} above pinch off voltage.
- Consequently, drain current remains constant. The characteristics resemble that of a pentode valve.

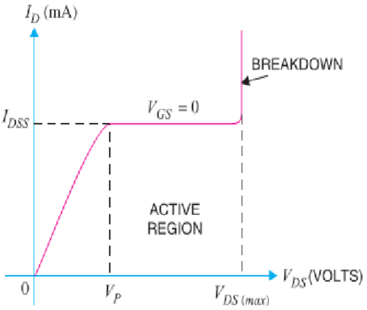


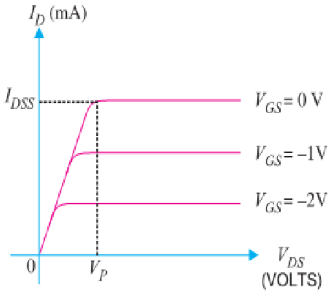
SALIENT FEATURES OF JFET : -

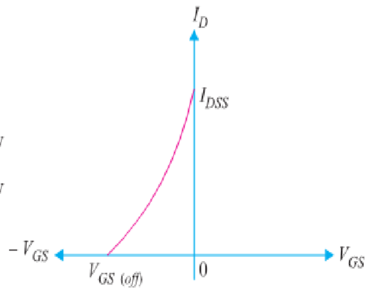
- The following are some salient features of JFET:
  - **(i)** A JFET is a three-terminal voltage-controlled semiconductor device i.e. input voltage controls the output characteristics of JFET.
  - **(ii)** The JFET is always operated with gate-source pn junction reverse biased.
  - **(iii)** In a JFET, the gate current is zero i.e. $I_G = 0A$. **(iv)** Since there is no gate current, $I_D = I_S$
  - **(v)** The JFET must be operated between V_{GS} and V_{GS} (off). For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.
  - **(vi)** As two gates are the same potential, both depletion layers widen or narrow by an equal amount.
  - **(vii)** The JFET is not subjected to thermal runaway when the temperature of the device increases.
  - **(viii)** The drain current I_D is controlled by changing the channel width.
  - **(ix)** Since JFET has no gate current, there is no β rating of the device. We can find drain current I_D

IMPORTANT TERMS : -









1. Shorted-Gate Drain Current (I_{DSS}): -

- It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is sometimes called zero-bias current.

2. Pinch Off Voltage (V_P) : -

- It is the minimum drain-source voltage at which the drain current essentially becomes constant.

3. Gate-Source Cut Off Voltage V_{GS} (off): -

- It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

PARAMETERS OF JFET: -

- Like vacuum tubes, a JFET has certain parameters which determine its performance in a circuit. The main parameters of JFET are: - **(i)** A.C. drain resistance **(ii)** Transconductance **(iii)** Amplification factor.
- **(i) A.C. Drain Resistance (r_d).** Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a JFET. It may be defined as follows :
- It is the ratio of change in drain-source voltage (ΔV_{DS})to the change in drain current(ΔI_D) at constant gate-source voltage i.e.

$$\boxed{\textbf{A.C. Drain Resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \textbf{ at constant } V_{GS}}$$

- For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then, a.c. drain resistance, $r_d = \frac{2V}{0.02\ mA} = 100\ k\Omega$
- Referring to the output characteristics of a JFET in Fig., it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat.
- Therefore, drain resistance of a JFET has a large value, ranging from 10 kΩ to 1 MΩ.
- **(ii) Transconductance (g_{fs}) : -** The control that the gate voltage has over the drain current is measured by transconductance g_{fs} & is similar to the transconductance g_m of the tube. It may be defined as follows :
- It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage(ΔV_{GS}) at constant drain-source voltage i.e.

$$\boxed{\textbf{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \textbf{ at constant } V_{DS}}$$

- The transconductance of a JFET is usually expressed either in mA/volt or micro mho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then, Transconductance,

  ➔ $g_{fs} = \frac{0.3\ mA}{0.1\ V} = 3mA/V = 3\times10^{-3}$ A/V or mho or S(Siemens)$=3\times10^{-3} \times 10^{6}\ \mu$ mho $= 3000\ \mu$ mho (or μS)

♣ **(iii) Amplification Factor (μ).** It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage(ΔV_{GS}) at constant drain current i.e.

$$\boxed{\textbf{Amplification Factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \textbf{ at constant } I_D}$$

- Amplification factor of a JFET indicates how much more control the gate voltage has over drain current than has the drain voltage.
- For instance, if the amplification factor of a JFET is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

❖ RELATION AMONG JFET PARAMETERS: -

- The relationship among JFET parameters can be established as under :

We know $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

- Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \quad \Rightarrow \quad \boxed{\mu = r_d \times g_{fs}}$$

➔ Amplification Factor = A.C. Drain Resistance × Transconductance

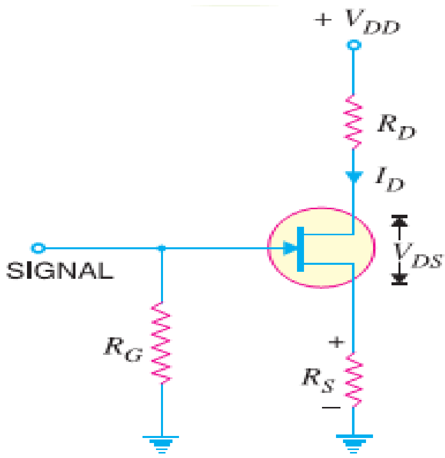
❖ JFET BIASING: -

- For the proper operation of n-channel JFET, gate must be negative w.r.t. source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit.
- The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery: - In this method, JFET is biased by a bias battery V_{GG}. This battery ensures that gate is always negative w.r.t. source during all parts of the signal.

2. Biasing circuit: -The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are **(i) Self-Bias (ii) Potential Divider Method**.

❖ SELF-BIAS FOR JFET : -



- Fig shows the self-bias method for n-channel JFET. The resistor RS is the bias resistor.
- The d.c. component of drain current flowing through R_S produces the desired bias voltage.

Voltage across R_S, $V_S = I_D R_S$

- Since gate current is negligibly small, the gate terminal is at d.c. ground i.e., $V_G = 0$.

$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S \quad$ or $\quad V_{GS} = -I_D R_S$

- Thus bias voltage V_{GS} keeps gate negative w.r.t. source.

Operating point: -

- The operating point (i.e., zero signals I_D & V_{DS}) can be easily determined. Since the parameters of the JFET are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS(off)}}\right)^2$$

Also $\quad V_{DS} = V_{DD} - I_D (R_D + R_S)$

- Thus d.c. conditions of JFET amplifier are fully specified i.e. operating point for the circuit is (V_{DS}, I_D).

Also, $\quad R_S = \frac{|V_{GS}|}{|I_D|}$

- Note that gate resistor R_G does not affect bias because voltage across it is zero.

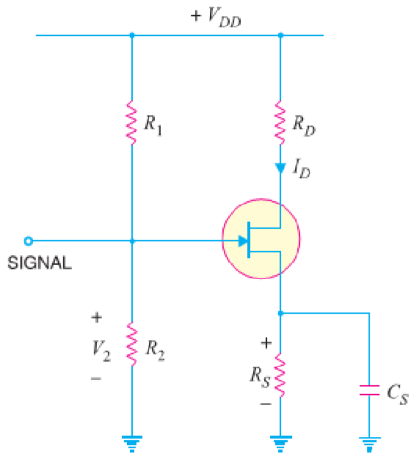
Midpoint Bias: - It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0.

- It can be proved that when $V_{GS} = V_{GS\,(off)} / 3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS}\left(1 - \frac{\Delta V_{GS}}{\Delta V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{\Delta V_{GS(off)}/3.4}{\Delta V_{GS(off)}}\right)^2 = 0.5\ I_{DSS}$$

- To set drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

❖ JFET with Voltage-Divider Bias :-



- Fig shows potential divider method of biasing a JFET. This circuit is identical to that used for a transistor.
- The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G) across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $V_2 = V_{GS} + I_D R_S$ Or $\mathbf{V_{GS} = V_2 - I_D R_S}$

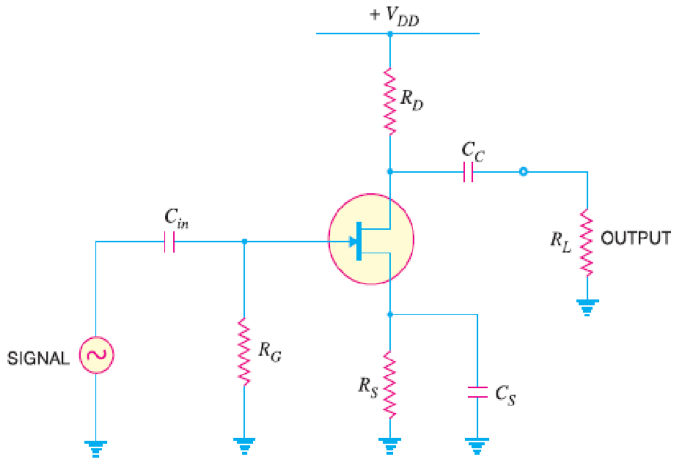
- The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:

$$I_D = \frac{V_2 - V_{GS}}{R_S} \quad \text{and} \quad V_{DS} = V_{DD} - I_D (R_D + R_S)$$

- Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point.
- The input impedance Z_i of this circuit is given by ; $Z_i = R_1 \parallel R2$

❖ JFET Connections: -

- There are three leads in a JFET viz., source, gate and drain terminals. However, when JFET is to be connected in a circuit, we require four terminals; two for the input and two for the output.
- This difficulty is overcome by making one terminal of the JFET common to both input and output terminals. Accordingly, a JFET can be connected in a circuit in the following three ways:
  - ♣ Common Source connection
  - ♣ Common Gate connection
  - ♣ Common Drain connection
- The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and moderate output impedance.



COMMON SOURCE CONNECTION

- However, the circuit produces a phase reversal i.e., output signal is 180° out of phase with the input signal. Fig. shows a common source n-channel JFET amplifier.
- Note that source terminal is common to both input and output.

JFET Applications : -

- The high input impedance and low output impedance and low noise level make JFET far superior to the bipolar transistor. Some of the circuit applications of JFET are :
  - ♣ As a Buffer amplifier
  - ♣ As Phase-shift oscillators
  - ♣ As RF amplifier

❖ Metal Oxide Semiconductor FET (MOSFET) :-

- The main drawback of JFET is that its gate must be reverse biased for proper operation of the device i.e.it can only have negative gate operation for n-channel and positive gate operation for p-channel.
- This means that we can only decrease the width of the channel (i.e. decrease the conductivity of the channel) from its zero-bias size.
- This type of operation is referred to as depletion-mode operation. Therefore, a JFET can only be operated in the depletion-mode.
- However, there is a field effect transistor (FET) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) i.e. it can have enhancement-mode operation. Such a FET is called **MOSFET.**
- A field effect transistor (FET) that can be operated in the enhancement-mode is called a **MOSFET**.
- A MOSFET is an important semiconductor device & can be used in any of the circuits covered for JFET.

- However, a MOSFET has several advantages over JFET including high input impedance and low cost.

❖ TYPES OF MOSFETS :-

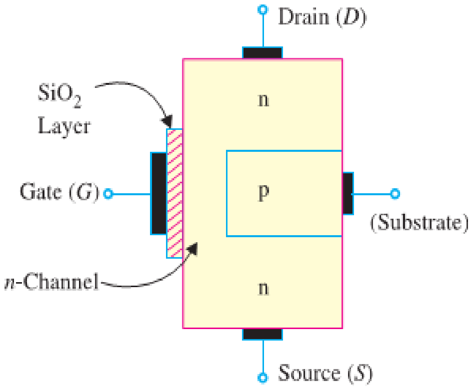
- There are two basic types of MOSFETs such as: -

1. Depletion-type MOSFET or D-MOSFET. The D-MOSFET can be operated in both the depletion mode and the enhancement-mode.
   - For this reason, a D-MOSFET is sometimes called **Depletion/Enhancement MOSFET**.

2. Enhancement-type MOSFET or E-MOSFET. The E-MOSFET can be operated only in enhancement mode. The manner in which a MOSFET is constructed determines whether it is D-MOSFET or E-MOSFET.

❖ **D-MOSFET.** Fig shows the constructional details of n-channel D-MOSFET.

- It is similar to n-channel JFET except with the following modifications/remarks :
- **(i)** The n-channel D-MOSFET is a piece of n-type material with a p-type region (called substrate) on the right and an insulated gate on the left as shown in Fig.

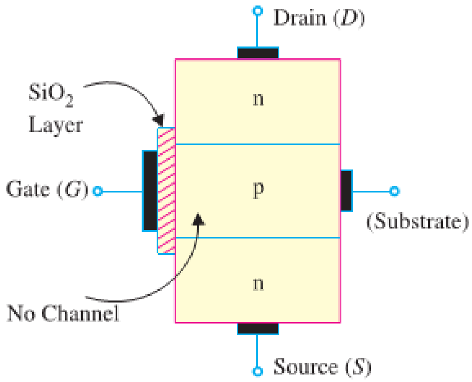


n-Channel D-MOSFET

- The free electrons (Q it is n-channel) flowing from source to drain must pass through the narrow channel between the gate and the p-type region (i.e. substrate).
- **(ii)** Note carefully the gate construction of D-MOSFET. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel.
- A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, thus gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and other plate is the channel with SiO_2 as dielectric. Recall that we have a gate diode in a JFET.
- **(iii)** It is a usual practice to connect the substrate to the source (S) internally so that a MOSFET has three terminals viz Source (S), Gate (G) and Drain (D).
- **(iv)** Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode. However, JFET can be operated only in depletion-mode.

❖ **E-MOSFET**. Fig shows the constructional details of n-channel E-MOSFET. Its gate construction is similar to that of D-MOSFET.

- The E-MOSFET has no channel between source and drain unlike the D-MOSFET. Note that the substrate extends completely to the SiO_2 layer so that no channel exists.



n-Channel E-MOSFET

- The E-MOSFET requires a proper gate voltage to form a channel (called induced channel). It is reminded that E-MOSFET can be operated only in enhancement mode.
- In short, the construction of E-MOSFET is quite similar to that of the D-MOSFET except for the absence of a channel between the drain and source terminals.

❖ Why the name MOSFET ?

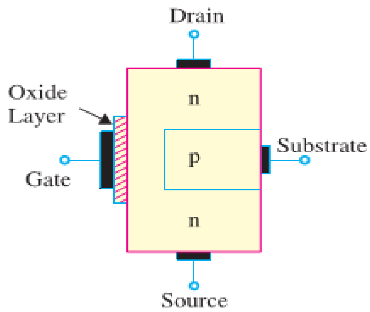
- The reader may wonder why is the device called MOSFET?
- The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor.
- Thus, going from gate to substrate, we have a metal oxide semiconductor and hence the name MOSFET.
- Since the gate is insulated from the channel, the MOSFET is sometimes called **insulated-gate FET** (IGFET). However, this term is rarely used in place of the term MOSFET.

❖ Symbols for D-MOSFET

There are two types of D-MOSFETs such as

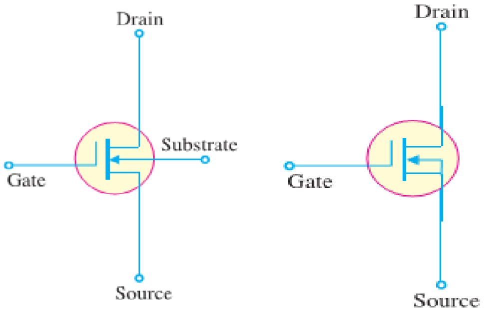
(i) n-channel D-MOSFET and **(ii)** p-channel D-MOSFET

- **(i) N-Channel D-MOSFET**. Fig (i) shows the various parts of n-channel D-MOSFET.



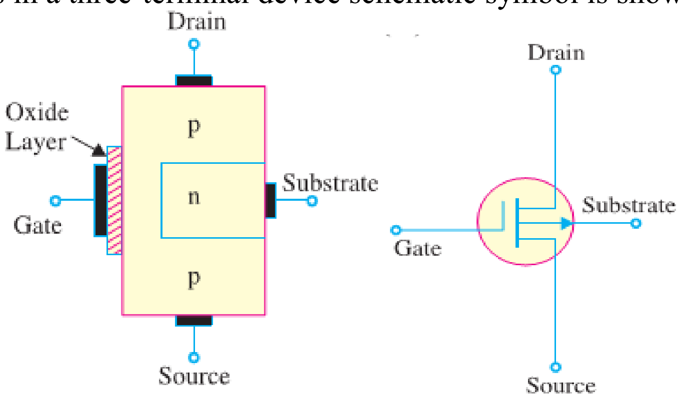
n-Channel D-MOSFET
(i)

- The p-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.
- Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel.
- The symbol for n-channel D-MOSFET is shown in Fig (ii).
- The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel.
- The drain lead comes out of the top of the channel and the source lead connects to the bottom.
- The arrow is on the substrate and points to the n-material; therefore we have n-channel D-MOSFET.
- It is a usual practice to connect substrate to source internally as shown in Fig. (iii).



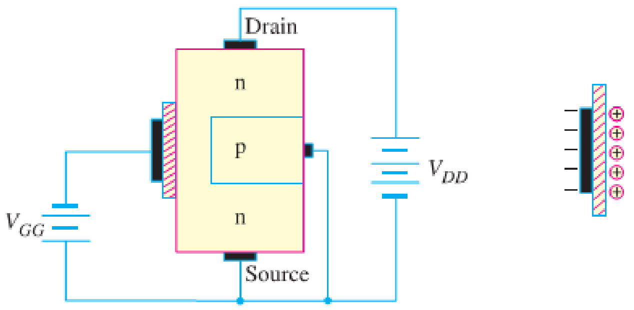
Symbol (ii) Symbol (iii)

- This gives rise to a three-terminal device.
- **(ii) P-Channel D-MOSFET.** Fig (i) shows the various parts of p-channel D-MOSFET.
- The n-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.
- The conduction takes place by the flow of holes from source to drain through this narrow channel.
- The symbol for p-channel D-MOSFET shown in Fig (ii). It is a usual practice to connect the substrate to source internally.
- This results in a three-terminal device schematic symbol is shown in Fig(iii).



p-Channel D-MOSFET (*i*) Symbol (*ii*) Symbol (*iii*)

❖ Circuit Operation of D-MOSFET



(*i*) (*ii*)

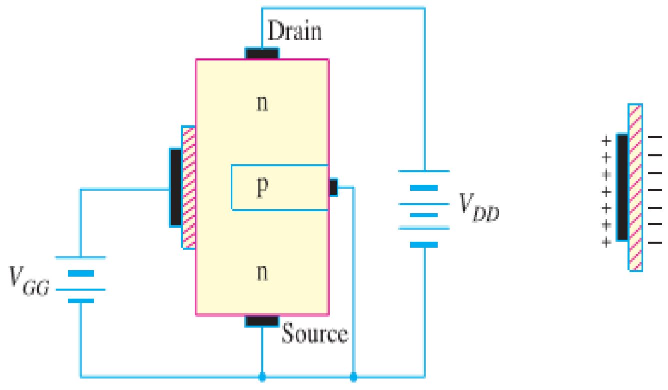
- Fig (i) shows the circuit of n-channel D-MOSFET. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric.
- When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel.
- Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate.
- The negative-gate operation is called **Depletion Mode** whereas positive gate operation is known as **Enhancement Mode**.

♣ **Depletion Mode**. Fig (i) shows depletion-mode operation of n-channel D-MOSFET. Since gate is negative, it means electrons are on the gate as shown is Fig (ii).

- These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel as shown in Fig (ii).
- In other words, we have depleted (i.e. emptied) the n-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the n- channel.

- This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.
- Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain.
- Note that with negative voltage to the gate, the action of D-MOSFET is similar to JFET.
- Because the action with negative gate depends upon depleting (i.e. emptying) the channel of free electrons, the negative-gate operation is called depletion mode.

♣ **(ii) Enhancement Mode.** Fig (i) shows enhancement-mode operation of n-channel D-MOSFET. Again, the gate acts like a capacitor.



(i) (ii)

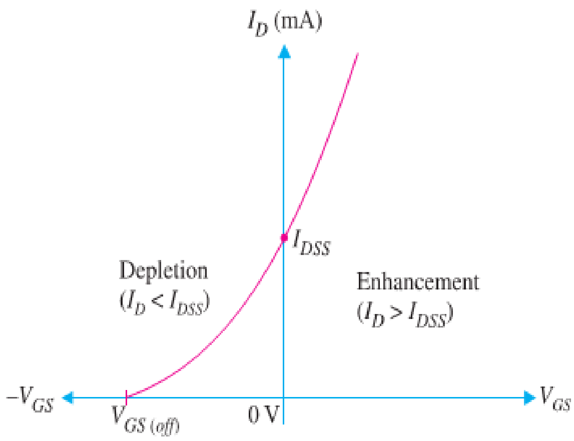
- Since the gate is positive, it induces negative charges in the n-channel as shown in Fig (ii).
- These negative charges are the free electrons drawn into the channel.
- Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased.
- Thus a positive gate voltage enhances or increases the conductivity of the channel.
- The greater the positive voltage on the gate, greater the conduction from source to drain.
- Thus by changing the positive voltage on the gate, we can change the conductivity of the channel.
- The main difference between D-MOSFET and JFET is that we can apply positive gate voltage to D-MOSFET and still have essentially zero current.
- Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.

♣ **The following points may be noted about D-MOSFET operation: -**

- **(i)** In D-MOSFET, source to drain current is controlled by electric field of capacitor formed at the gate.
- **(ii)** The gate of JFET behaves as a reverse-biased diode whereas the gate of a D-MOSFET acts like a capacitor. For this reason, it is possible to operate D-MOSFET with positive or negative gate voltage.
- **(iii)**As the gate of D-MOSFET forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate.
- For this, the input impedance of D-MOSFET is very high, ranging from 10,000 MΩ to 10, 000, 00 MΩ.
- **(iv)** The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the D-MOSFET has, therefore, a very low input capacitance.
- This characteristic makes the D-MOSFET useful in high-frequency applications.

❖ D-MOSFET Transfer Characteristic : -

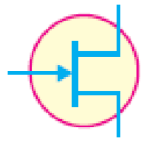
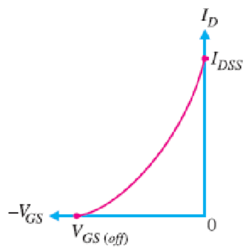
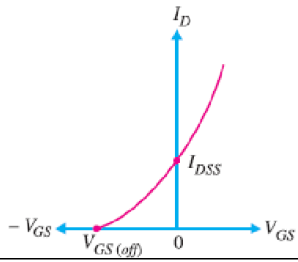
- Fig shows the transfer characteristic curve (or transconductance curve) for n-channel D-OSFET.
- The behaviour of this device can be beautifully explained with the help of this curve as under :-



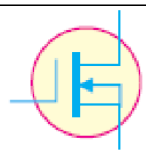
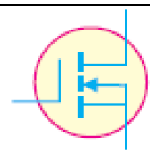
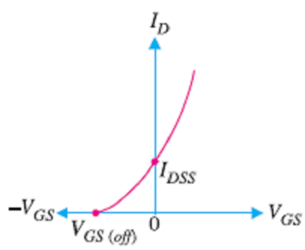
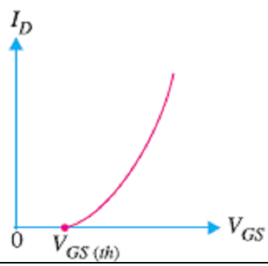
- **(i)** The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted i.e. $V_{GS} = 0$.
- (ii) As V_{GS} goes negative, I_D decreases below value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS(off)}$ just as with JFET.
- **(iii)**When V_{GS} is positive, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of D-MOSFET.
- Note that the transconductance curve for the D-MOSFET is very similar to the curve for a JFET.
- Because of this similarity, the JFET and the D-MOSFET have the same transconductance equation viz.

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2}$$

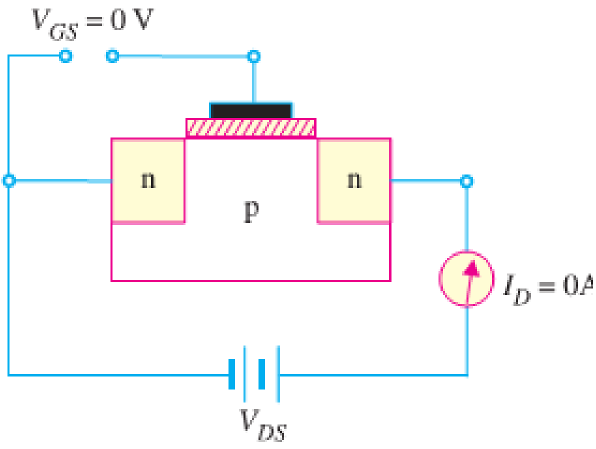
❖ D-MOSFET Vs JFET: -

SN	Parameters	JFETs	D-MOSFETs
1	Symbol		
2	Transconductance Curve		
3	Modes of operation:	Depletion only	Depletion and enhancement
4	Commonly Used bias circuits:	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias;	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias; **(4)** Zero bias
5	Advantages:	Extremely high input impedance.	**(1)** Higher input impedance than a comparable *JFET*. **(2)** Can operate in both modes (Depletion and Enhancement).
6	Disadvantages:	**(1)**Bias instability; **(2)** Can operate only in depletion mode.	**(1)** Bias instability. **(2)** More sensitive to changes in temperature than the *JFET*.

❖ Table below summarizes many of the characteristics of D-MOSFETs and E-MOSFETs: -

SN	Parameters	D-MOSFETs	E-MOSFETs
1	Symbol		
2	Transconductance Curve		
3	Modes of Operation:	Enhancement and Depletion	Enhancement Only
4	Commonly Used bias circuits:	**(1)** Gate bias; **(2)** Self bias; **(3)** Voltage-divider bias; **(4)** Zero bias.	**(1)** Gate bias; **(2)** Voltage-divider bias; **(3)** Drain-feedback bias.

❖ E-MOSFET: -



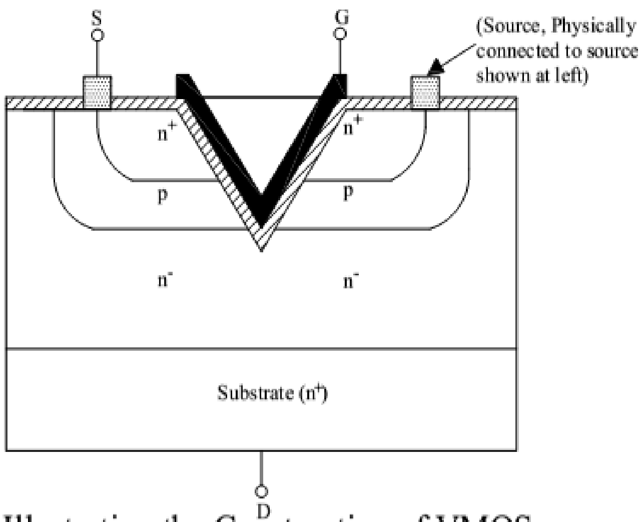
- Two things are worth noting about E-MOSFET.
- First, E-MOSFET operates only in the enhancement mode and has no depletion mode.
- Secondly, the E-MOSFET has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig (i)].
- It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting.
- The minimum value of V_{GS} of proper polarity that turns on E-MOSFET is called **Threshold voltage** [$V_{GS\,(th)}$].
- The n-channel device requires positive V_{GS} ($\geq V_{GS\,(th)}$) & the p-channel device requires negative V_{GS} ($\geq V_{GS\,(th)}$).

❖ Power MOSFETs: -

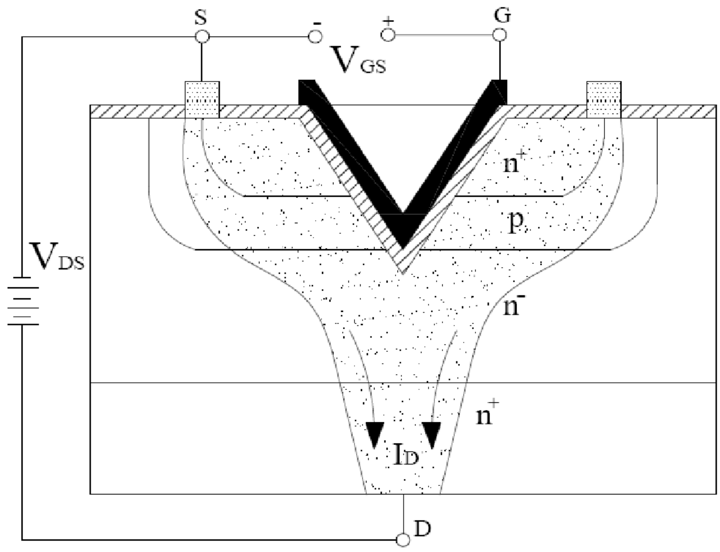
- With the advancement of technology, the engineers have produced a wide variety of MOSEFTs that are designed specifically for high current, high voltage and high power applications.
- Some Examples of Power MOSFET are VMOS, LDMOS etc.

❖ VMOS [V-Grove MOSFET or Vertical MOSFET] :-

- One of the major disadvantages of a typical MOSFET is the reduced power handling level as compared to BJT transistors. The power handling level of a typical MOSFET is less than 1W.
- This drawback of the MOSFET can be overcome by changing the construction mode from one of the planer nature to one with a vertical structure as shown in Fig.



Illustrating the Construction of VMOS



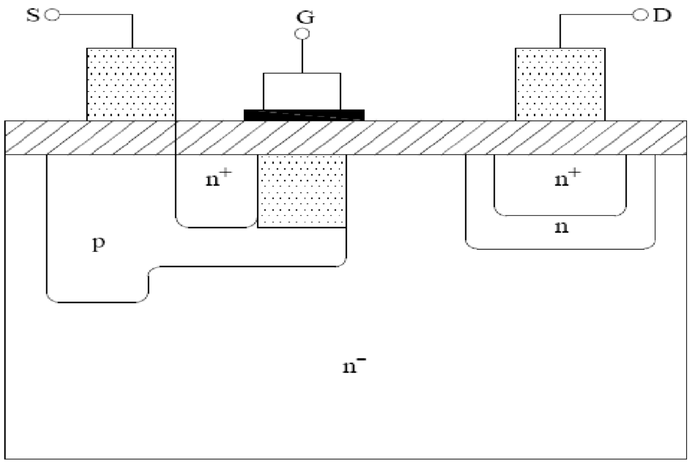
[Illustrating VMOS Operation]

- As seen from this figure, all the elements of the planar MOSFET are present in the vertical metal-oxide silicon FET (or simply VMOS) the metallic surface connection to the terminals of the device.
- The vertical-MOSEFT (or simple VMOS) is a component designed to handle much larger drain currents than the standard MOSEFT.
- The current handling capability of the VMOS is a result of its physical construction which is illustrated in Fig. As seen from this figure, the component gas materials that are labelled as P, N^+ and N^-.
- The N^- material labels indicate differences in doping levels.
- Also notice that there is no physical channel connecting the source (at top) and the drain (at bottom). Thus VMOS is an *enhancement type* MOSEFT.
- With V-shaped gate, a larger channel is formed by a positive gate voltage.
- With a large channel, the device is capable of handling large amount of drain current.
- The Operation of VMOS is illustrated in Fig.

VMOS Operation: -

- When a positive gate voltage is applied to the device, an N-type channel forms in the P-type regions. This effective channel connects the source to the drain.
- As seen from the figure the shape of the gate causes a wider channel to form than is created in the standard MOSFET. Hence, the amount of drain current is much higher for this component.
- Moreover, the VMOS can exhibit a higher transconductance and a lower turn-on resistance than the conventional planer MOSFET.
- Another advantages of using VMOS id the fact it is not susceptible to thermal runaway.
- The VMOS has a positive temperature coefficient, means that the resistance of the component increases when temperature increases.
- Thus an increase in temperature will cause a decrease in drain current.
- The VMOS device can be fabricated with more than one V-grove to increase amount of drain current and some other performance characteristics.

LD MOS: -



LDMOS

- The LDMOS (i.e. Lateral Double Diffused MOSFET) is another type of power MOSFET.
- This MOSFET uses a very small channel region and a heavily doped N-type region (N^+) to obtain a high drain current and low channel resistance [$r_{d(ON)}$].
- Fig shows the basic construction of LDMOS.
- As seen from this figure, the narrow channel (Shaded region) is made up of the P-type material that lies between the N^- Substrate (lightly doped) and the N^+ (heavily doped) source region.
- Since only the N-type material lies between the channel and the drain, the effective length of the channel is externally short. This coupled with the N-type material in channel-to-drain path provides an extremely low value of $r_{d\,(ON)}$.
- With a low channel resistance, the LDMOS device can handle very high amount of current without generating and damaging amount of heat.
- The LDMOS has typical values of $r_{d\,(ON)}$ that are in the range of 2Ω or less.
- With this low value channel resistance, it is typically capable of handling current as high as 20 A.

C-MOS: -

- C-MOS means complementary MOS. These are mostly used in the field of digital electronics to manufacture logic gates and many other synchronous and asynchronous circuits.
- The logic gates includes AND, OR & NOT gates and their various combinations.
- The synchronous circuit includes flip-flops, counters, memories, A/D and D/A converters.
- The asynchronous circuit includes combinations of logic gates such as decoders, encoders, multiplexers and de-multiplexers etc.
- A CMOS logic circuit consists of combinations of NMOS & PMOS devices.

[CHAPTER-5]

[FEED BACK AMPLIFIER]

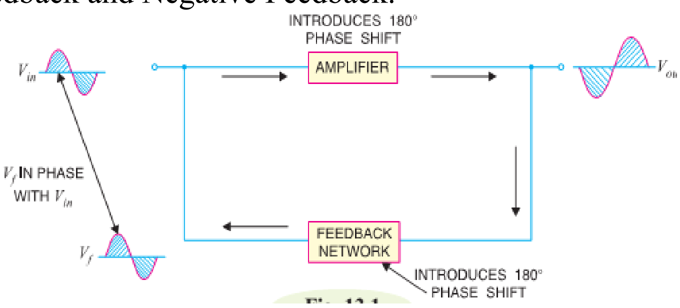
❖ INTRODUCTION:-

- A practical amplifier has a gain of nearly one million i.e. its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output.
- The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of negative feedback i.e. by injecting a fraction of output in phase opposition to the input signal.
- The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

❖ FEEDBACK:-

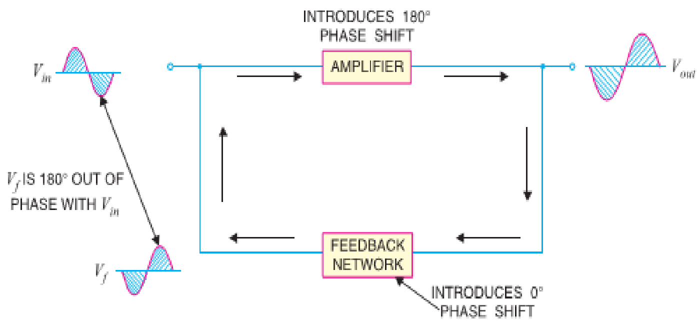
- The process of injecting a fraction of output energy of some device back to the input is known as **feedback.** Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers viz Positive Feedback and Negative Feedback.

Positive Feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback*. This is illustrated in Fig.



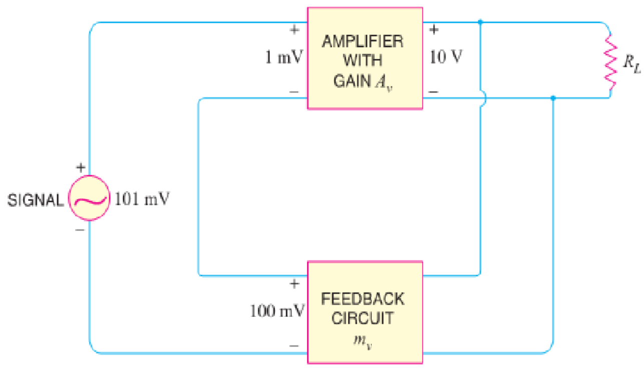
- Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage V_f to be in phase with the input signal V_{in}.
- The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is not often employed in amplifiers.
- One important use of positive feedback is in oscillators. If positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative Feedback. When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback*. This is illustrated in Fig.



- As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage V_f is 180° out of phase with the input signal V_{in}.
- Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances.
- It is due to these advantages that negative feedback is frequently employed in amplifiers.

❖ PRINCIPLES OF NEGATIVE VOLTAGE FEEDBACK IN AMPLIFIERS:-



- A feedback amplifier has main two parts such as an amplifier and a feedback circuit.
- The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input.
- Fig. shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative.
- The output of the amplifier is 10 V. The fraction m_v of this output i.e.100 mV is feedback to the input where it is applied in series with the input signal of 101 mV.
- As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier.