

Discipline :- ETC	Semester:- 5 <sup>TH</sup>	Name of the Teaching Faculty:-Anchal Sundar Ray
Subject:-VLSI & EMBEDDED SYSTEM	No of Days/per Week Class Allotted :- 04	Semester From:- <u>15/09/2022</u> To:- <u>22/12/2022</u>
Week	Class Day	Theory
1 <sup>ST</sup>	1	Historical perspective- Introduction
	2	Classification of CMOS digital circuit types
	3	Introduction to MOS Transistor& Basic operation of MOSFET.
	4	Structure and operation of MOSFET (n-MOS enhancement type)
2 <sup>nd</sup>	1	Structure and operation of cmos
	2	MOSFET V-I characteristics,
	3	Working of MOSFET capacitances.
	4	Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level -3 model
3 <sup>rd</sup>	1	Flow Circuit design procedures
	2	VLSI Design Flow & Y chart
	3	Design Hierarchy
	4	VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom
4 <sup>th</sup>	1	Simplified process sequence for fabrication
	2	Basic steps in Fabrication processes Flow
	3	Fabrication process of n-MOS Transistor
	4	CMOS n-well Fabrication Process Flow

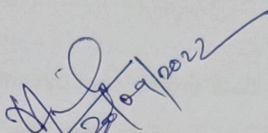
5 <sup>th</sup>	1	MOS Fabrication process by n-well on p-substrate
	2	
	3	CMOS Fabrication process by P-well on n-substrate
	4	
6 <sup>th</sup>	1	Layout Design rules
	2	Stick Diagrams of CMOS inverter
	3	Basic n-MOS inverters
	4	Working of Resistive-load Inverter
7 <sup>th</sup>	1	Inverter with n-Type MOSFET Load
	2	Enhancement Load,
	3	Depletion n-MOS inverter
	4	CMOS inverter – circuit operation
8 <sup>th</sup>	1	characteristics and interconnect effects: Delay time
	2	CMOS Inverter design with delay constraints
	3	Two sample mask lay out for p-type substrate
	4	Define Static Combinational logic
9 <sup>th</sup>	1	working of Static CMOS logic circuits (Two-input NAND Gate)
	2	Introduction to Dynamics logic circuits & Memories
	3	CMOS logic circuits ( NAND2 Gate)
	4	CMOS Transmission Gates(Pass gate)

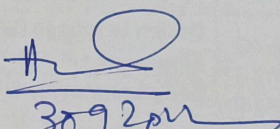
10 <sup>th</sup>	1 <sup>st</sup>	Complex Logic Circuits - Basics
	2 <sup>nd</sup>	Classification of Logic circuits based on their temporal behaviour
	3 <sup>rd</sup>	
	4 <sup>th</sup>	SR Flip latch Circuit,
11 <sup>th</sup>	1 <sup>st</sup>	Clocked SR latch only.
	2	CMOS D latch.
	3 <sup>rd</sup>	
	4 <sup>th</sup>	Basic principles of Dynamic Pass Transistor Circuits
12 <sup>th</sup>	1 <sup>st</sup>	Dynamic RAM, SRAM,
	2 <sup>nd</sup>	Flash memory
	3 <sup>rd</sup>	Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xilinx
	4 <sup>th</sup>	Design strategies & concept of FPGA with standard cell based design
13 <sup>th</sup>	1 <sup>st</sup>	VHDL for design synthesis using CPLD or FPGA
	2 <sup>nd</sup>	Raspberry Pi - Basic idea
	3 <sup>rd</sup>	Embedded Systems Overview
	4 <sup>th</sup>	list of embedded systems, characteristics ,example – A Digital Camera
14 <sup>th</sup>	1 <sup>st</sup>	Embedded Systems Technologies--Technology – Definition
	2 <sup>nd</sup>	Technology for Embedded Systems, Processor Technology , IC Technology
	3 <sup>rd</sup>	Design Technology-Processor Technology,General Purpose Processors – Software
	4 <sup>th</sup>	Basic Architecture of Single Purpose Processors – Hardware



15 <sup>th</sup>	1 <sup>st</sup>	Application – Specific Processors, Microcontrollers, Digital Signal Processors (DSP)
	2 <sup>nd</sup>	IC Technology- Full Custom / VLSI, Semi-Custom ASIC (Gate Array & Standard Cell)
	3 <sup>rd</sup>	PLD (Programmable Logic Device)
	4 <sup>th</sup>	PLD (Programmable Logic Device)

Anchal Sunder  
Teaching Faculty  
30.09.2022

  
HOD, ETC

  
Principal

Government Polytechnic, dhenkanal  
Principal  
Govt. Polytechnic  
Dhenkanal