LECTURE NOTES ON

ANALOG ELECTRONICS & LINEAR IC

4TH SEMESTER ETC

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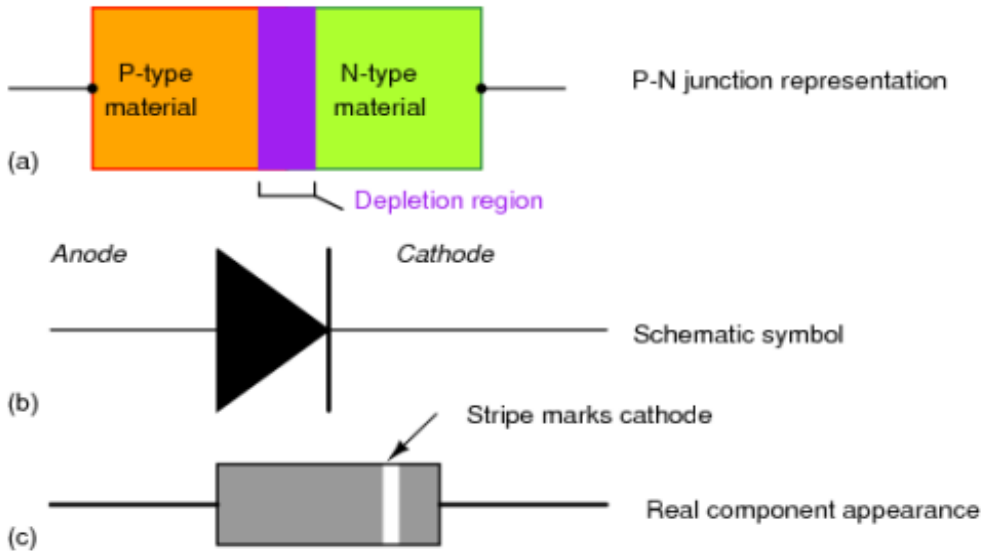
UNIT-I: DIODE TRANSISTORS AND CIRCUITS

PN-JUNCTION :

- When a p-type & n-type material are suitably joined the contact region is called pn-junction.
- PN-junction is very important for manufacturing different electronic devices , like rectifier,LED, Zener diode.
- Structure :



PROPERTIES OF PN-JUNCTION

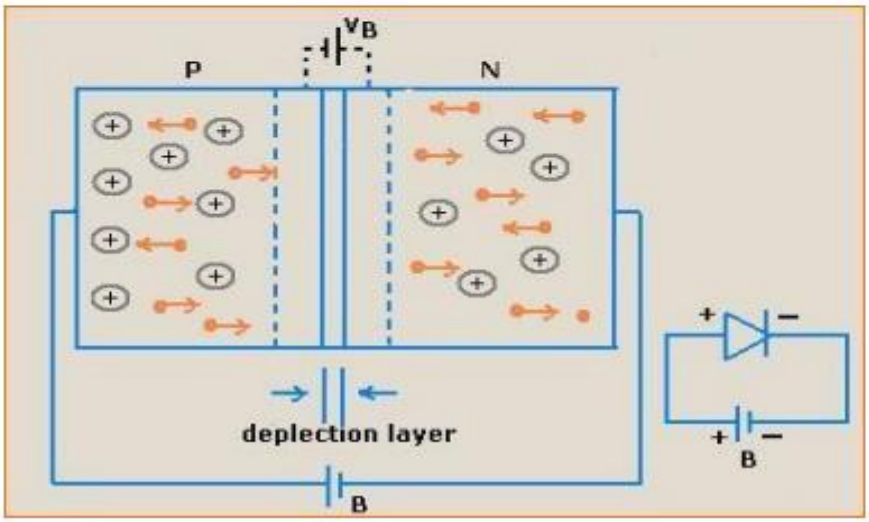
- The p-type material has majority holes & minority free electrons .Each hole is associatedby a –ve ion. Similarly the n-type material has majority free electrons & minority holes.
  Each free electrons is associated by +ve ion.

- When this p-type & n-type material are joined to form pn-junction, at the junction the +vehole on p-side & the –ve free electron on n-side attract each other & cancel after combination.Due to this combination a net –ve charge develops on p-side & net +ve charge

- The region across which barrier potential exist is called depletion layer, because this layeris depleted of charge carrier.

WORKING PRINCIPLE OF PN JUNCTION :

* For proper operation of pn-junction an external supply should be used. The external supply magnitude should be greater than barrier potential & applied in forward condition i.e. +ve terminal is connected to p-type & -ve to n-type as shown in figure below :



*If there is no external voltage applied across the pn-junction, a barrier potential exists across the junction & due to this the pn-junction is not conducting & current through pn-junction is zero.

*When external voltage is applied, the majority holes in p-type are repelled by the +ve terminal of the source & free electrons in n-type are repelled by the –ve terminal of the sources. As an result both free electrons & holes move towards the junction & cancels barrier potential. This movement produces current flow through the pn-junction.

*It is clear from the figure that current flow inside the pn-junction is due to two types of charge carrier, i.e. free electrons & holes, but outside the junction current is due to only free electrons.

BIASING OF PN JUNCTION :

*The process of applying external voltage across the pn-junction is called biasing.

*Types of biasing :

a) Zero bias

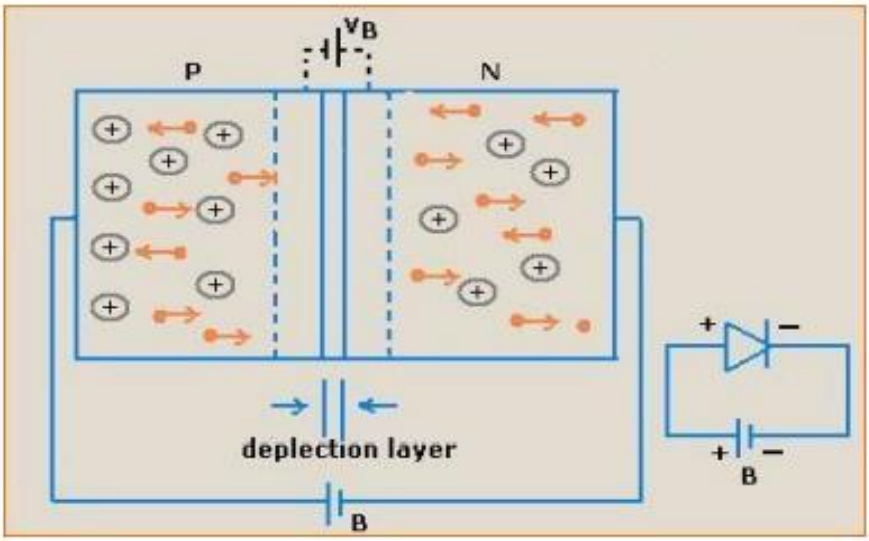
b) Forward bias

c) Reverse bias

Zero Bias: The pn-junction without any external supply is called zero bias. Under this condition the pn-junction is not conducting due to existence of barrier potential.

Forward Bias

- If p-type material is connected to +ve & n-type to –ve of external supply, yhe pn-junction issaid to be forward bias.
- FIGURE :

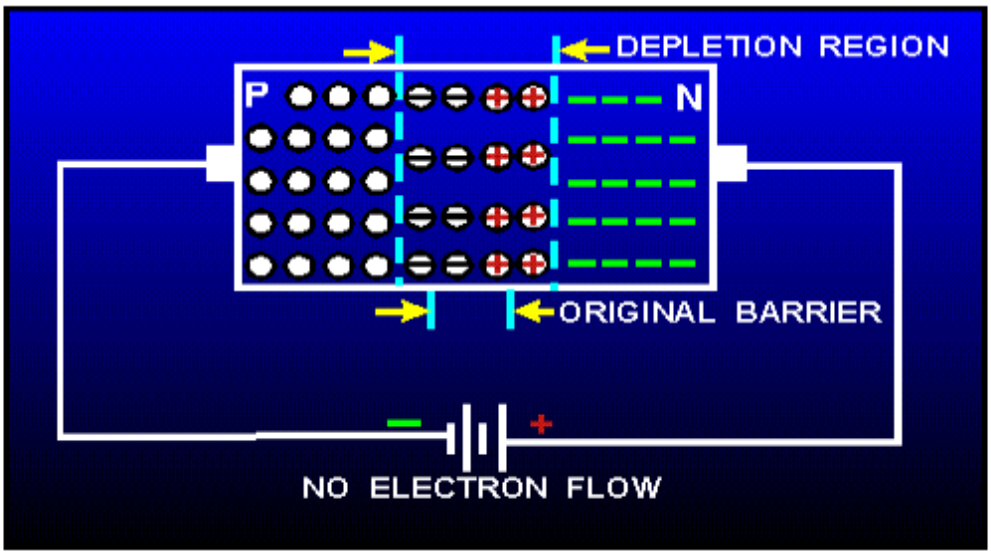


- Due to forward biasing the +ve terminal of external supply repels the holes towards the junction. Similarly the majority free electrons in n-region repelled by the –ve terminal of thesupply. As a result there is a continuous movement of free electrons & holes across the junction. The pn-junction is now conducting.
- It is clear from the figure that current inside the pn-junction is due to two types of chargecarriers, that is free electrons & holes, but out side the junction current is due to only free electrons.
- Due to forward biasing the barrier potential is eliminated. Depletion width decreases.

  Due to forward biasing resistance of pn-junction decreases & conductivity increases.

Reverse Biasing

- When p-type is connected to –ve & n-type to +ve of external supply the pn-junction is saidto be reverse biased.
- Figure :



- Under reverse biased condition the majority holes of p-type are attracted by -ve terminal ofthe supply & majority free electrons of n-type are attracted by +ve terminal of supply. As a result the majority free electrons & holes are moving away from the junction. No majority carriers cross the junction. The PN-junction is said to not conducting & no current flow through the pn-junction.
- Due to minority carrier very small current , in the range of micro ampere flows across thepn-junction. This small minority current sometimes assumed as approximately zero.
- Due to reverse biasing the resistance of pn-junction increases & conductivity decreases tovery small value.
- Due to reverse biasing depletion width increases. The barrier potential actsin the same direction as the external supply . Hence it can not be cancelled.

V~I CHARACTERISTIC OF PN-JUNCTION :

- The graph which shows the relation between voltage applied across a pn-junction & currentflowing through it is called V~I characteristic.

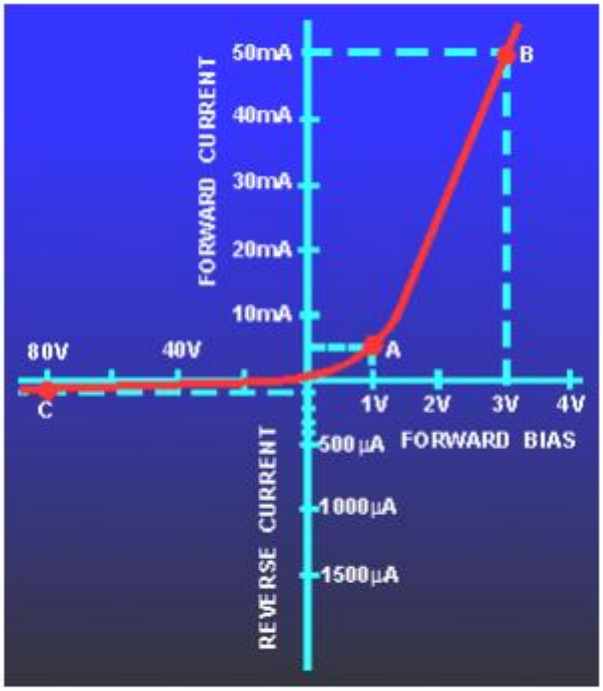
- Two types of V~I characteristic :

  a) Forward V~I characteristic

  b) Reverse V~I characteristic

Forward V~I Characteristic :

- The characteristic under forward bias condition of pn-junction is called forwardcharacteristic.
- By changing the position of variable resistor R number of readings are taken from voltmeter& ammeter. All readings are plotted on a graph paper & the resulting graph is called forward V~I characteristic.
- Graph:



- When the voltage across the pn-junction is zero, no current flows. If we increase the voltageacross pn-junction in forward direction, at first current increases very slowly with voltage, but after certain voltage, current increases very rapidly with voltage. This voltage is called Knee voltage.
- Below Knee voltage current is very small due to barrier potential, because supply voltage istrying to cancel the barrier potential. But after knee voltage, barrier potential completely cancelled & current rises very rapidly.

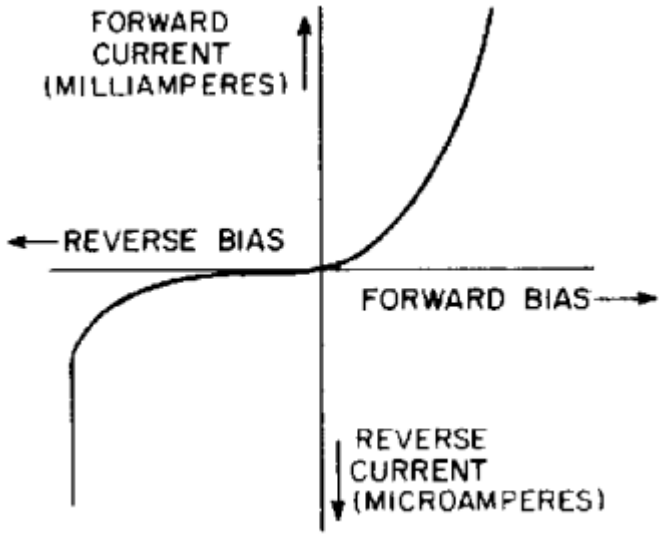
REVERSE CHARACTERISTIC:

- The characteristic under reverse condition of pn-junction is called reverse characteristic.

- The characteristic can be drawn by taking readings for different position of variable resistor.
- If the voltage increases from zero to onwards in –ve direction, at first current rises veryslowly with voltage. This process continues upto a certain voltage known as avalanche breakdown voltage VB.
- At VB current suddenly increases to a very high value.
- Above break down voltage if voltage across pn-junction increases further, then it has noeffectover the current .

At break down voltage the pn-junction may burnt due to excess heat.

Complete V~I Characteristic:

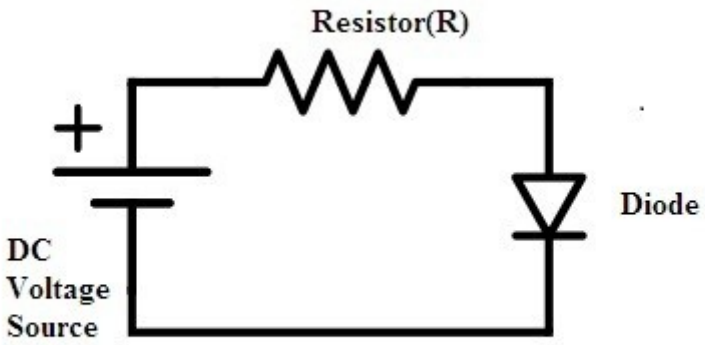


DC Load Line of a Diode and Its Equation

DC load line for a non-linear device is drawn by making the reactive components as zero. Hence a diode is considered as a non-linear device and its voltage and current characteristics are exponentially related to each other. The formation of the intersection point for the characteristic curve and the straight line or dc-load line can be analyzed better by considering the example for the diode as in forward bias condition.

Let us consider a diode connected to the resistor(R), source of voltage (V_{DD}) in series. The diode is connected in forward bias so that the forward current and the forward voltages flowing through the circuit. As per the Kirchhoff's current law, the current flowing through the diode (I_D) and the resistor (I_R) is equal.

Analysis of the circuit is done by applying Kirchhoff's voltage law (KVL). This law results in the formation of the final equation for the dc load line. Here the dc voltage is the biasing voltage of the circuit by keeping any further reactive components as zero.



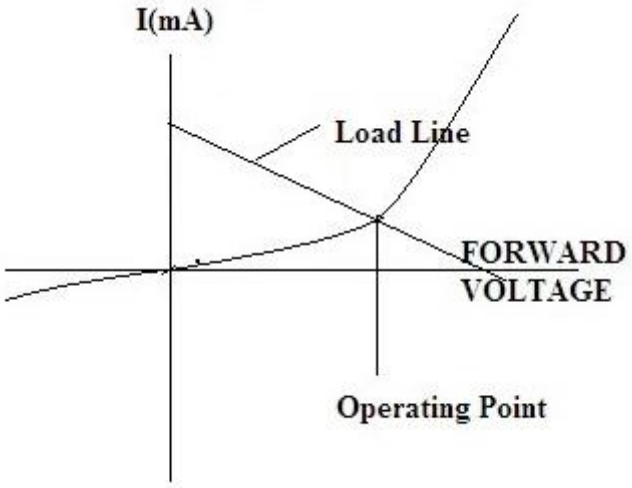
diode-operating-in-forward-bias-for-the-analysis-of-dc-load

$V_{DD} = V_D + I_D R$

$V_D = I_D R - V_{DD}$

Where V_{DD}, is the applied dc source voltage and V_D is the voltage across the diode. Hence the above can be considered as the equation for the diode. The voltage and current characteristics of the diode in forward bias condition can be drawn. By our previous analysis on the condition of the diode in forward bias applied a voltage and the generated current in the circuit are exponentially related to each other.

After a certain cut-off voltage, the diode starts operating in forward bias condition. To this slope, the technique is considered and a straight line on the v-i characteristics is drawn. The slope here for the above general circuit for the diode is V_{DD}/R.



IMPORTANT TERMS: -

(i)BREAKDOWN VOLTAGE: - It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.

(ii)KNEE VOLTAGE: - It is the forward voltage at which the current through the junction starts to increase rapidly.

(iii) PEAK INVERSE VOLTAGE (PIV):- It is the maximum reverse voltage that can be applied to the pn junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service.

(iv)MAXIMUM FORWARD CURRENT:- It is the highest instantaneous forward current that a pn junction can conduct without damage to the junction. Manufacturer‘s data sheet usually specifies this rating. If the forward current in a pn junction is more than this rating, the junction will be destroyed due to overheating.

Diode Break Down:

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction :

1. ***avalanche breakdown*** **and**
2. ***Zener breakdown.***

Avalanche breakdown **and**

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.*

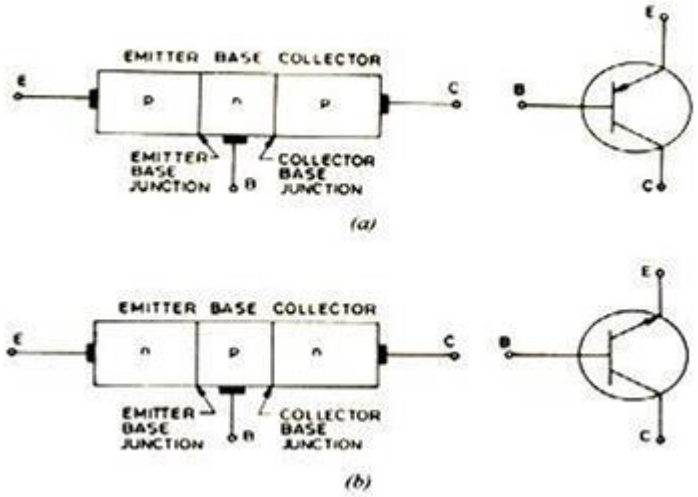
Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 10^7 V/m.

TRANSISTOR:

The electronic device in which a dissimilar type of semiconductor material is sandwiched between two similar type of semiconductor is called transistor. In this either a p-type is sandwiched between two n-type or an n-type is sandwiched between two p-type material. Transistor consists of two words: transistor. **Trans** means the signal transfer property of the device & **istor** means resistor property of the device. A transistor transfers a signal from a low resistance to high resistance.

TYPES OF TRANSISTOR: There are two types of transistors: a)n-p-n transistor b)p-n-p transistor Structure¬ & Symbol:



It has three terminals, one taken from each type of semiconductor. The terminals are named as¬ base(B), emitter(E), collector(C). It has two pn-junction¬ & three semiconductor layers. TERMINALS OF TRANSISTOR: It has three terminals, named as base, emitter & collector. The two end terminals are known as emitter(E) & collector(C), middle is called as base.

Emitter

a)This layer provides charge carriers.

b)It is always forward biased w.r.t. base.

c) It is wider than base.

d)It is heavily doped. Hence it provides large numbers of charge carriers into base.

Base:

a)This layer controls the amount of charge carrier flow from emitter to collector.

b)It is forward connected w.r.t. emitter & reverse biased w.r.t. collector.

c)It is much thinner than emitter.

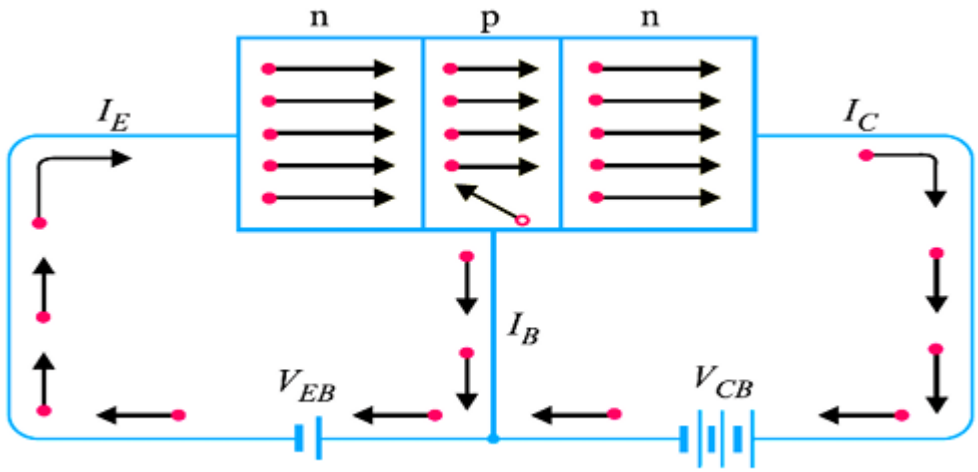
d)It is lightly dopped. Hence it passes most of the charge carriers coming from emitter to collector.
Collector:

a)This layer removes charges from its junction with the base.

b)It is reverse biased w.r.t. base. c)It is wider than emitter & base.

d)It is moderately doped.

WORKING PRINCIPLE OF NPN TRANSISTOR: *Figure shows the circuit for showing the working principle.



Basic connection of *npn* transistor

*For proper operation of transistor, base emitter junction is forward biased by V_{EE} & base-collector is reverse biased by V_{CC}.
*The n-type emitter has majority free electrons. The forward bias on emitter, causes the free electrons in the n-type emitter to flow towards the base.This constitutes the emitter current I_E.
*When the free electrons flows through p-type base, they try to combine with majority holes in base resion. Since the base is lightly doped & very thin, only a few electrons combine with holes & constitute base current I_B.
*The remaining free electrons flows towards the collector attracted by strong positive terminal of the biasing supply $+V_{cc}$. This constitute the collector current I_C.
*It is clear that almost the entire emitter current flows in the collector circuit. Hence emitter current is the sum of collector & base current i.e.

$$I_E=I_B+I_C$$

*The current conduction within the transistor is due to free electrons & also through the external circuit is due to free electrons.

*For proper operation of transistor, base emitter junction is forward biased by V_{EE} & base-collector is reverse biased by V_{CC}.

*The p-type emitter has majority holes. The forward bias on emitter, causes the holes in the p-type emitter to flow towards the base.This constitutes the emitter current I_E.

*When the holes flows through n-type base, they try to combine with majority free electrons in base resion. Since the base is lightly doped & very thin, only a few holes combine with free electrons & constitute base current I_B.

*The remaining holes flows towards the collector attracted by strong negative terminal of the biasing supply $-V_{cc}$. This constitute the collector current I_C.

*It is clear that almost the entire emitter current flows in the collector circuit. Hence emitter current is the sum of collector & base current i.e.

$$I_E=I_B+I_C$$

*The current conduction within the transistor is due to holes & through the external circuit is due to free electrons.

TRANSISTOR CONNECTION:

There are three types of connections:

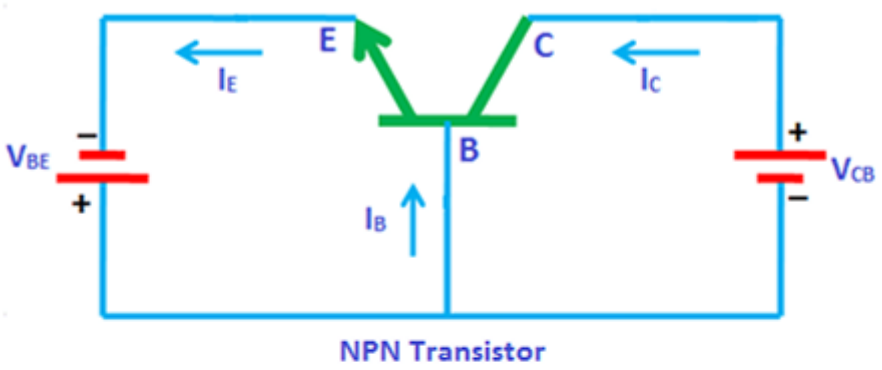
a) Common- Base Connection(CB)
b) Common-Emitter Connection(CE)
c) Common-Collector Connection(CC)

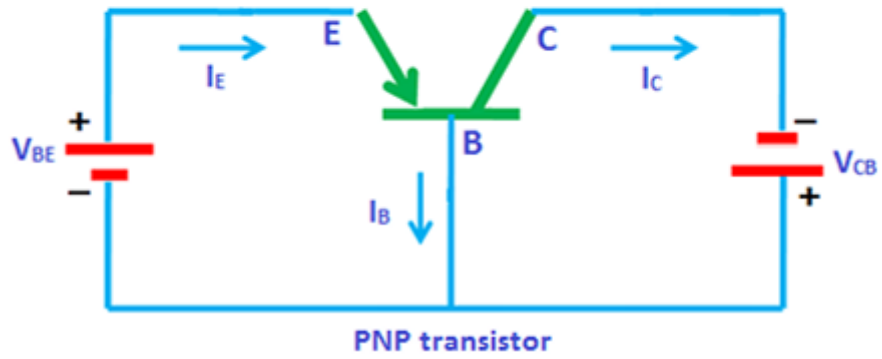
COMMON-BASE CONNECTION:

* The transistor connection in which base is common for both input & output circuit is called common-base connection.

*In this input is applied between emitter & base & output is taken from collector & base.

*Circuit Diagram:





Common base configuration

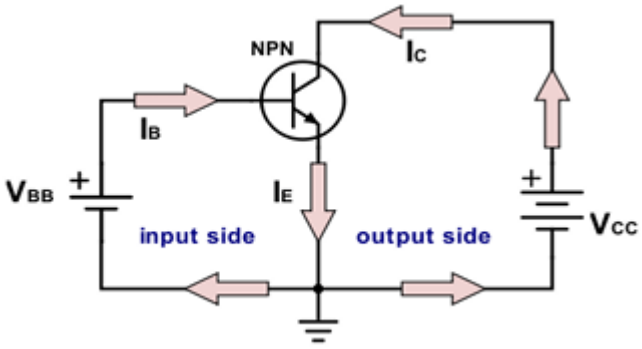
*D.C. supply V_{EE} provides forward biasing & V_{cc} provides reverse biasing.

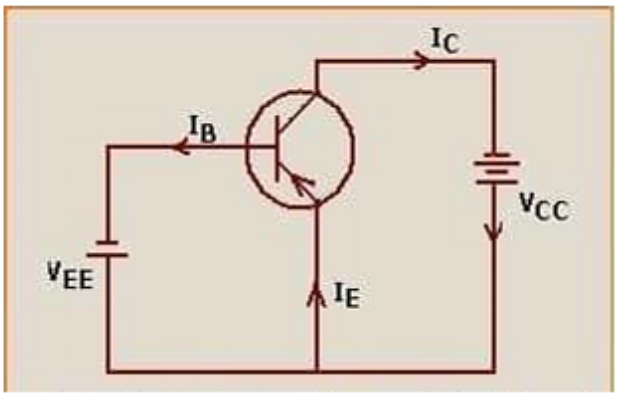
COMMON-EMITTER CONNECTION

* The transistor connection in which emitter is common for both input & output circuit is called common-emitter connection.

*In this input is applied between emitter & base & output is taken from collector & emitter.

*Circuit Diagram:





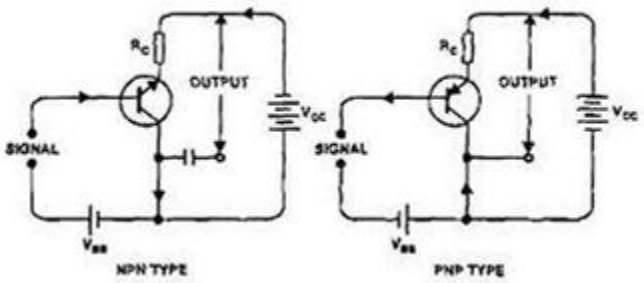
*D.C. supply V_{BB} provides forward biasing & V_{cc} provides reverse biasing.

COMMON-COLLECTOR CONNECTION:

* The transistor connection in which collector is common for both input & output circuit is called common-collector connection.

*In this input is applied between base & collector & output is taken from collector & emitter.

*Circuit Diagram:



*D.C. supply V_{BB} provides forward biasing across base to collector & V_{cc} provides reverse biasing across emitter to collector.

CURRENT AMPLIFICATION FACTOR IN COMMON BASE CONNECTION(α):

*The ratio between change in collector current to change in emitter current at constant collector to base voltage V_{CB} is called current amplification factor α.

*Mathematically, $\alpha=\Delta I_C/\Delta I_E$ at constant V_{CB}

*Its value is less than unity. Practical values of α ranges from 0.9 to 0.99.

CURRENT AMPLIFICATION FACTOR IN COMMON EMITTER (β):

*The ratio between change in collector current to change in base current at constant collector to emitter voltage V_{CE} is called current amplification factor β.

*Mathematically, $\beta=\Delta I_C/\Delta I_B$ at constant V_{CE}

*Its value is greater than 20. Practical values of β ranges from 20 to 500.

CURRENT AMPLIFICATION FACTOR IN COMMON COLLECTOR(Y)

*The ratio between change in emitter current to change in base current at constant collector to emitter voltage V_{CE} is called current amplification factor β.

*Mathematically, $Y=\Delta I_E/\Delta I_B$ at constant V_{CE}

*Its value is greater than 20. Practical values of β ranges from 20 to 500 i.e. same as common emitter value.

RELATION BETWEEN α & β:

We know $\beta=\Delta I_C/\Delta I_B$ ……(1)

$\alpha=\Delta I_C/\Delta I_E$ ……(2)

$I_E=I_B+I_C$

$\Delta I_E=\Delta I_B+\Delta I_C$

Hence $\Delta I_B=\Delta I_E-\Delta I_C$

Substituting the values of ΔI_B in equation (1), we get,

$\beta=\Delta I_C / \Delta I_E-\Delta I_C$ ……..(3)

Dividing both numerator & denominator by ΔI_E of R.H.S. in eqn.(3),

$\beta=(\Delta I_C/ \Delta I_E)/ (\Delta I_E/ \Delta I_E)-(\Delta I_C/ \Delta I_E)=\alpha/(1-\alpha)$

$\beta=\alpha/1-\alpha$

RELATION BETWEEN Y & α:

We know

$Y=\Delta I_E/\Delta I_B$ ……(4)

$\alpha=\Delta I_C/\Delta I_E$ ……(5)

$\Delta I_E=\Delta I_B+\Delta I_C$

Hence $\Delta I_B=\Delta I_E-\Delta I_C$

Substituting the value of ΔI_B in eqn. (4),

$Y=\Delta I_E/\Delta I_B= \Delta I_E/ \Delta I_E-\Delta I_C$ ……..(6)

Dividing both numerator & denominator by ΔI_E of eqn. (6),

$Y=\Delta I_E/\Delta I_B= (\Delta I_E/ \Delta I_E)/(\Delta I_E/ \Delta I_E)-(\Delta I_C /\Delta I_E)=1/1-\alpha$

$Y=1/1-\alpha$

RELATION BETWEEN α, β & Y:

We know

$\alpha=\Delta I_C/\Delta I_E$ ……..(7)

$\beta=\Delta I_C /\Delta I_B$ ……(8)

$Y=\Delta I_E/\Delta I_B$ ……(9)

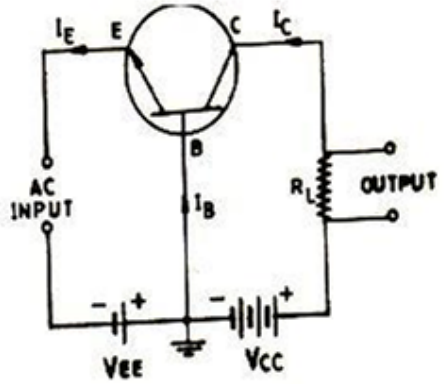
Multiplying $\Delta I_E / \Delta I_E$ in R.H.S. of eqn. (8),

$\beta=(\Delta I_C /\Delta I_B)x (\Delta I_E/ \Delta I_E)= (\Delta I_C /\Delta I_E)x (\Delta I_E/ \Delta I_B)=\alpha .Y$

$\beta= \alpha .Y$

COMMON BASE TRANSISTOR AMPLIFIER:

*Circuit diagram



*Circuit Details:

It consists of transistor Q, load resistor R_l , biasing supply V_{EE} & V_{CC}.

Transistor Q used for amplification. Amplified output develops across load resistor Rl.

V_{EE} provides proper forward biasing across emitter to base.

V_{CC} provides proper reverse biasing across collector to base.

Vi is the input supply to be amplified.

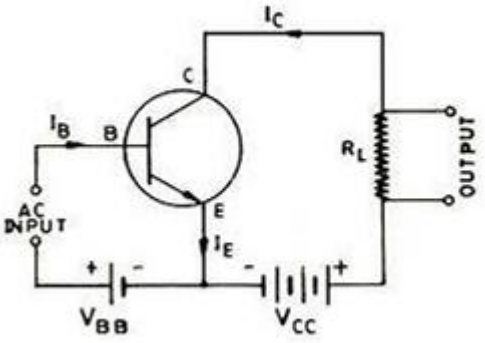
Vo is the amplified output.

*Circuit operation:

When the input signal to be amplified is applied across the emitter to base, for a small change in input we get a large change in output current. This large change in current when flows through a high load resistance Rl, produces a large voltage drop across Rl. Now if we compare the input voltage & output voltage, output is more than the input. In this way we get amplified output.

COMMON EMITTER AMPLIFIER:

*Circuit diagram:



*Circuit details:

It consists of transistor Q, load resistor R_l , biasing supply V_{BB} & V_{CC}.

Transistor Q used for amplification. Amplified output develops across load resistor Rl.
V_{BB} provides proper forward biasing across emitter to base.
V_{CC} provides proper reverse biasing across collector toemitter.
V_i is the input supply to be amplified.
V_o is the amplified output.

*Operation:
1)During the positive half cycle of the input signal , forward bias across the emitter-base junction is increased. Hence more electrons flow from the emitter to the collector through the base. This causes an increase in collector current. The increased collector current when flows through a high load resistance R_l, produces high voltage drop.
2) During the negative half cycle of the input signal, the forward bias across emitter-base junction is decreased. Hence collector current decreases. This decreased collector current when flows through load resistance, produces decreased output voltage in opposite direction. Hence an amplified output is obtained across the load.

V-I CHARACTERISTIC OF COMMON BASE TRANSISTOR CONNECTION:

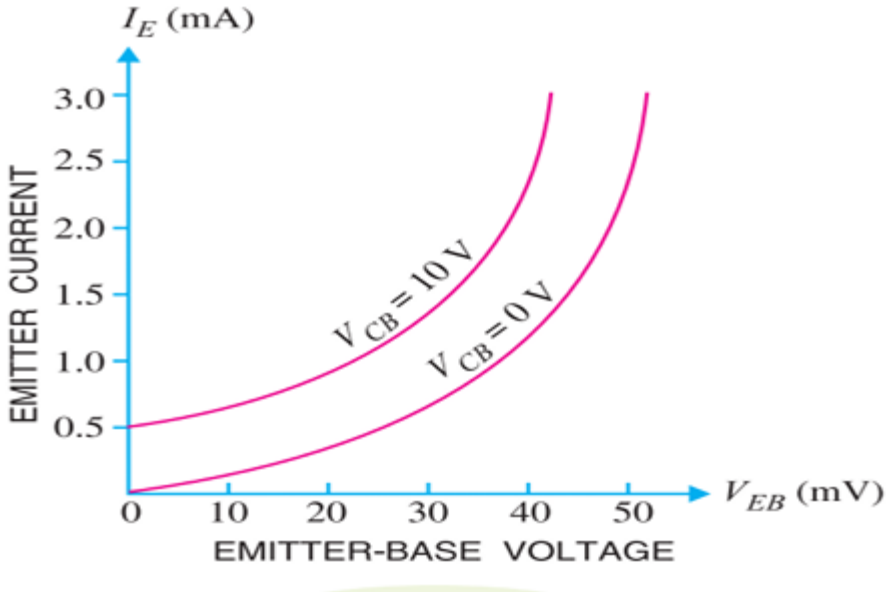
Two types of V-I characteristic,

a)Input V-I characteristic
b)Output V-I characteristic

INPUT V-I CHARACTERISTIC OF CB:

*The graph which shows the relation between emitter current I_E & emitter-base voltage V_{EB} at constant collector-base voltage V_{CB} is called input characteristic.
*V_{EB} is taken along x-axis & I_E is taken along y-axis.

*Graph:



*It is clear from the graph that , emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}.

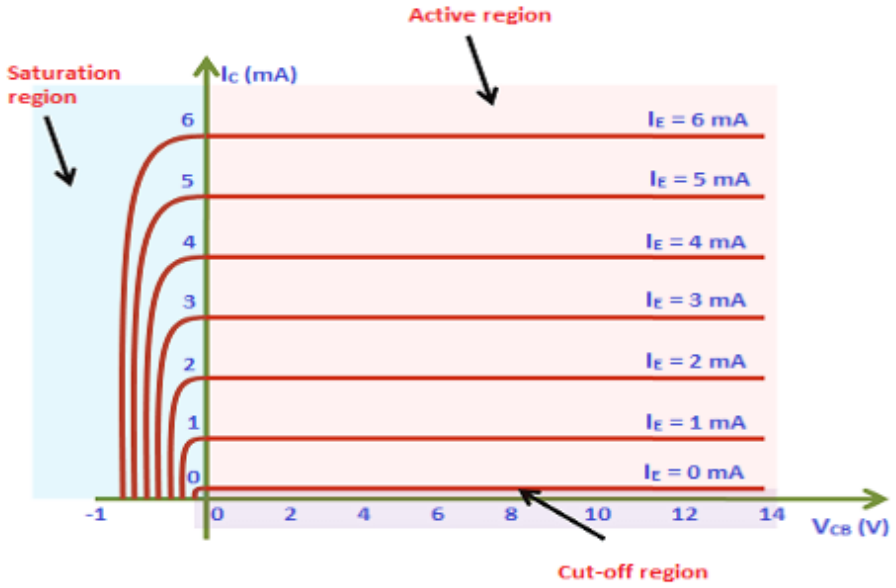
*The emitter current is almost independent of collector-base voltage V_{CB}.

OUTPUT V-I CHARACTERISTIC OF CB:

*The graph which shows the relation between collector current I_c & collector-base voltage V_{CB} at constant emitter current I_E is called output characteristic.

*V_{CB} is taken along x-axis & I_c is taken along y-axis.

*Graph:



O/P characteristics CB configuration

*It is clear from the graph that,

a) Collector current I_C varies with V_{CB} only at very low voltage(<1V).

b) For V_{CB} greater than 1V, collector current remains constant.

c) A very large change in collector-base voltage produces only a small change in collector current.

V-I CHARACTERISTIC OF COMMON-EMITTER CONNECTION:

There are two types of V-I characteristic:

1) Input V-I Characteristic

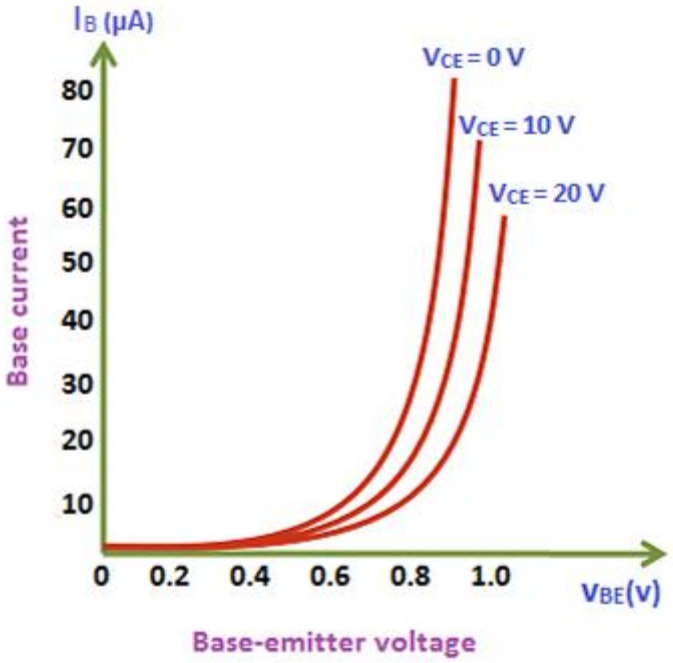
2) Output V-I characteristic

INPUT V-I CHARACTERISTIC OF CE:

*The graph which shows the relation between base current I_B & base-emitter voltage V_{BE} at constant collector emitter voltage V_{CE} is called input characteristic.

*V_{BE} is taken along x-axis & I_B is taken along y-axis.

*Graph:



I/P characteristics CE configuration

*It is clear from the graph that,

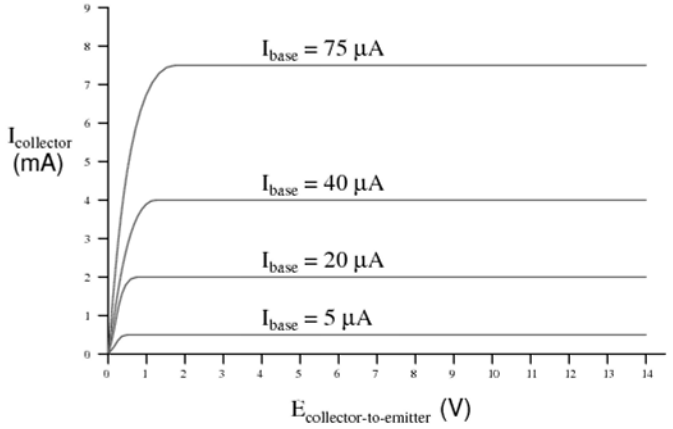
a) The characteristic is similar to characteristic of forward biased pn-junction.

b) At first current IB increases very slowly. After certain voltage known as knee voltage, the current increases rapidly.

OUTPUT V-I CHARACTERISTIC OF CE:

*The graph which shows the relation between collector current I_c & collector-emitter voltage V_{CE} at constant base current I_B is called output characteristic.

*V_{CE} is taken along x-axis & I_c is taken along y-axis.



- It is clear from the graph that,

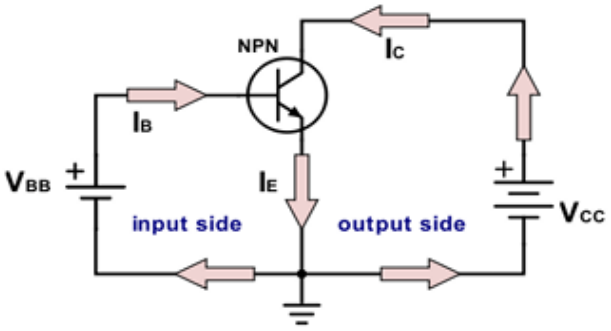
a)Collector current I_C varies with V_{CE} only at very low voltage(<1V).

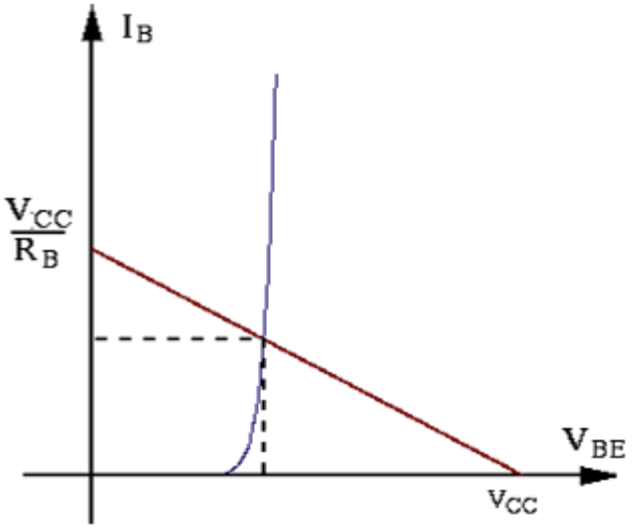
b)For V_{CE} greater than 1V, collector current remains constant.

c)A very large change in collector-emitter voltage produces only a small change in collector current.

TRANSISTOR DC LOAD LINE:

- It is a method of measuring collector current I_C for different values of collector-emitter voltage accurately.
- Circuit for getting dc load line:





- Appling output KVL:

$V_{CC}=V_{CE}+I_CR_C$

$V_{CE}=V_{CC}-I_CR_C$ ……..(10)

This equation is in the form of a straight line. Hence its graph is a straight line & can be drawn on output characteristics. The graph can be drawn as follows:

a)If $I_C=0$, then equation (10) is: $V_{CE}=V_{CC}$

This forms the coordinate $(V_{CE},I_C)=(V_{CC},0)$.This point is indicated by the point A on V_{CE} axis.

b)Putting $V_{CE}=0$ in eqn. (10):

$$0=V_{CC}-I_CR_C$$

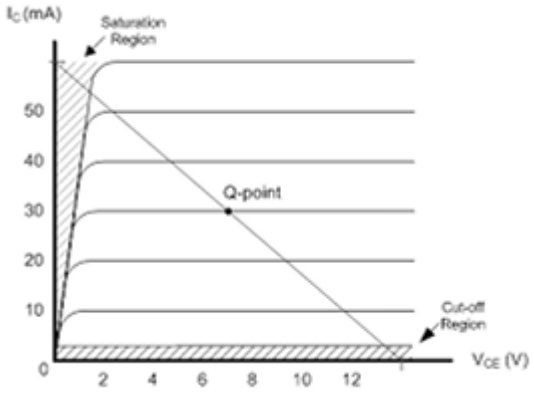
i.e. $I_C=V_{CC}/R_C$

This forms the coordinate $(V_{CE},I_C)=(0,V_{CC}/R_C)$.This point is indicated by the point B on I_C axis.

By joining the points A & B, the straight line AB is called dc load line.

OPERATING POINT:

- The zero signal values of collector current I_C & collector –emitter voltage V_{CE} is called operating point.
- The intersection of output V-I characteristic & dc load line is also called operating point.
- Also named as Q-point or quiescent point.



IMPORTANT SITUATIONS OF TRANSISTOR:

a)CUT OFF:

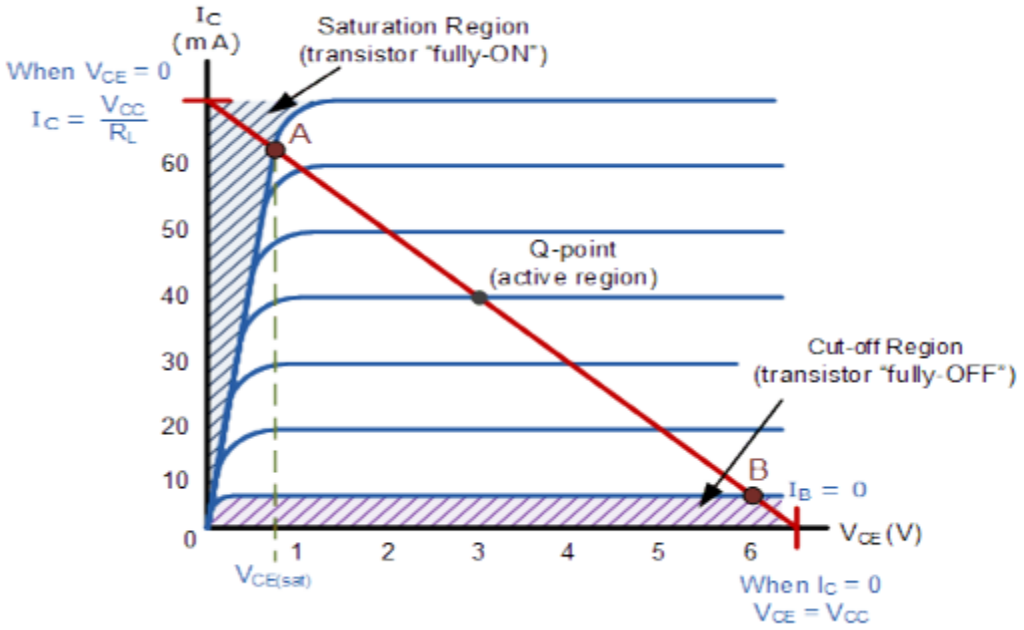
The point where the load line intersects the $I_B=0$ curve is known as cut off. The region below this point is called cut off region.

At cut off both input & output side is reverse biased & transistor action is lost.

b)Saturation : The point where the load line intersects the $I_B=I_B(sat)$ curve is called saturation .The region above this is called saturation region.

At saturation both input & output side is forward biased & normal transistor action is lost.

c)ACTIVE REGION: The region between cut off & saturation is called active region. In this region input is forward biased & output is reverse biased. The transistor action is normal.



S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

UNIT-V

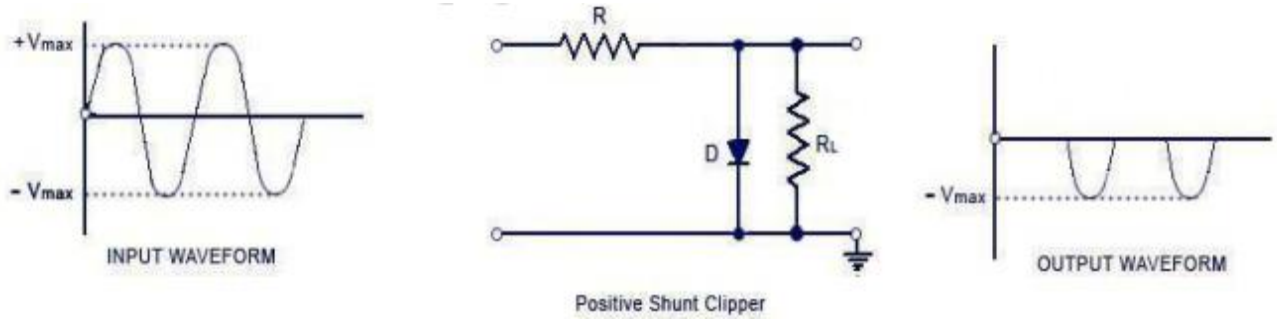
TUNED AMPLIFIER &WAVE SHAPING CIRCUIT

CLIPPING CIRCUITS

The circuit with which the waveform is shaped by removing (or clipping) a portion of theapplied wave¬ is known as a clipping circuit. Clippers find extensive use in radar, digital and other electronic systems. Although several clipping circuits have been developed to change the wave shape, we concentrate only on diode clippers. These clippers can remove signal voltages above or below a specified level. The important diode clippers are:- 1. Positive clipper and negative clipper 2. Biased positive clipper and biased negative clipper 3. Combination clipper.

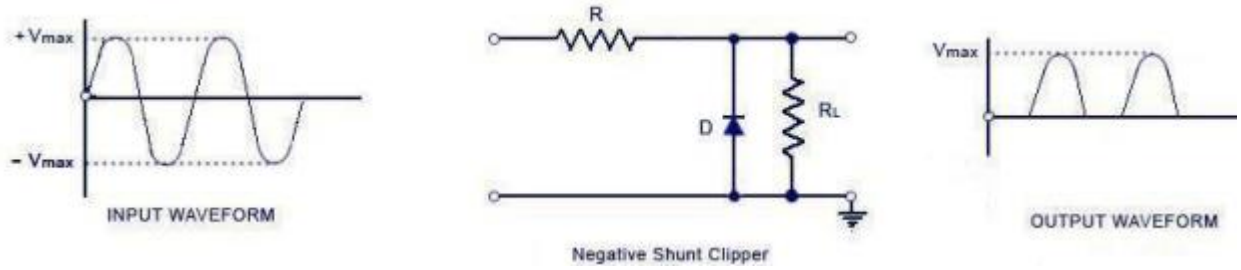
POSITIVE CLIPPER: A positive clipper is that which removes the positive half-cycles of the input voltage. The positive clipper is of two types¬ 1. Positive series clipper.

2. Positive shunt clipper The below Fig. shows the typical circuit of a positive shunt clipper using a diode¬



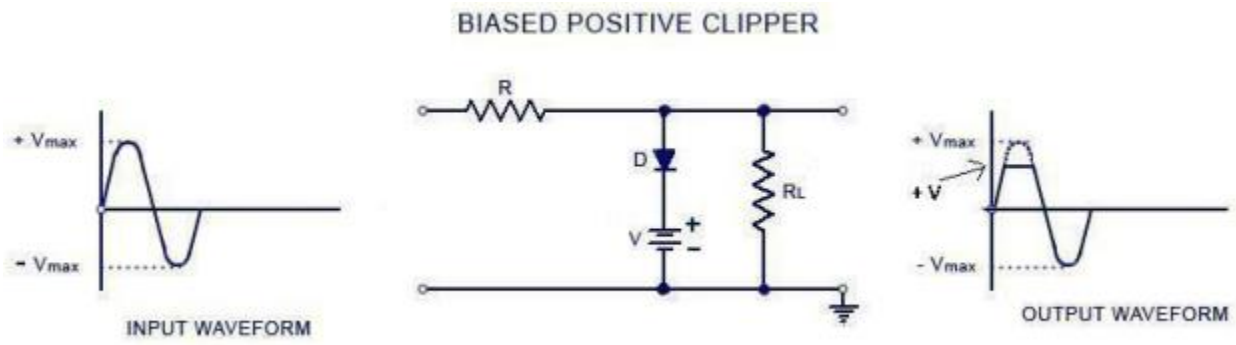
Here the diode is kept in parallel with the load. During the positive half cycle, the diode ⎯D is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance RL to be zero. Thus output voltage during the positive half cycles is zero. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance RL if R is much smaller than RL Actually the circuit behaves as a voltage divider with an output voltage of -[RL / R+ RL] Vmax ≅ -Vmax (Taking or assuming when RL >> R).

NEGATIVE CLIPPER: A negative clipper is that which removes the positive half-cycles of the input voltage.The negative clipper is of two types 1. Negative series clipper 2. Negative shunt clipper The below Fig. shows the typical circuit of a negative shunt clipper using a diode.



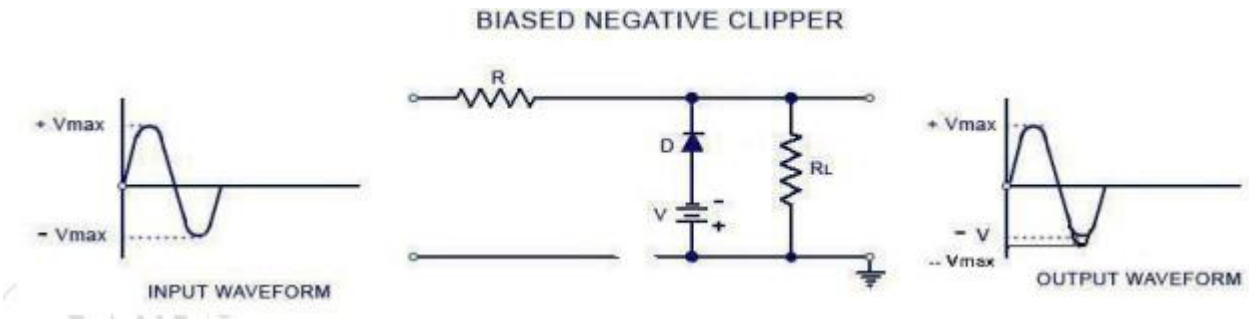
During the negative half cycle, the diode D is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop across the diode or across the load resistance RL to be zero. Thus output voltage during the negative half cycles is zero. During the positive half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently the entire input voltage appears across the diode or across the load resistance RL if R is much smaller than RL Actually the circuit behaves as a voltage divider with an output voltage of [RL / R+ RL] Vmax ≅ Vmax (¬ Taking or assuming when RL >> R).

BIASED POSITIVE CLIPPER When a small portion of the positive half cycle is to be removed, it is called a biased positive clipper.



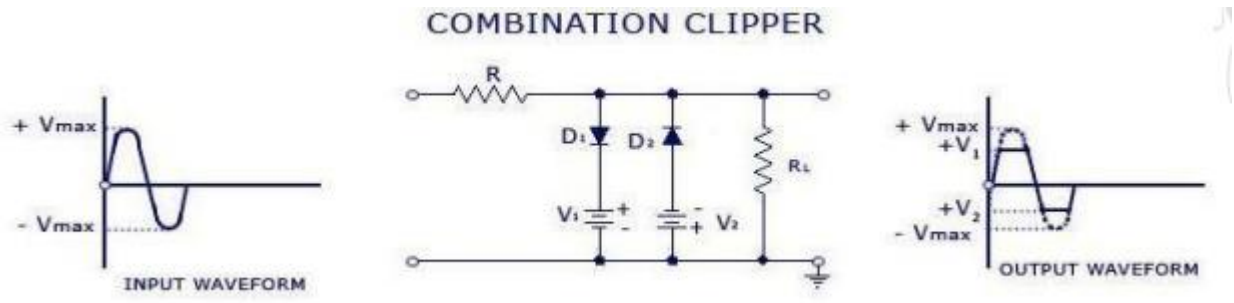
The circuit diagram and waveform is shown in the figure below. During negative half cycle, when the input signal voltage is negative, the diode _D is reverse-biased. This causes it to act as an open-switch. Thus the entire negative half cycle appears across the load, as illustrated by output waveform. During positive half cycle, when the input signal voltage is positive but does not exceed battery the voltage _V‘, the diode D remains reverse-biased and most of the input voltage appears across the output. When during the positive half cycle of input signal, the signal voltage becomes more than the battery¬ voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to + V‘ and stays at _+ V‘ as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, _V‘. Thus a biased positive clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

BIASED NEGATIVE CLIPPER When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper.



The circuit diagram and waveform is shown in the figure below. During positive half cycle, when the input signal voltage is positive, the diode _D' is reverse-biased. This causes it to act as an open-switch. Thus the entire positive half cycle appears across the load, as illustrated by output waveform. During negative half cycle, when the input signal voltage is negative but does not exceed battery the voltage _V', the diode _D' remains reverse-biased and most of the input voltage appears across the output. When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to _-V'and stays at _-V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, _V'. Thus a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage.

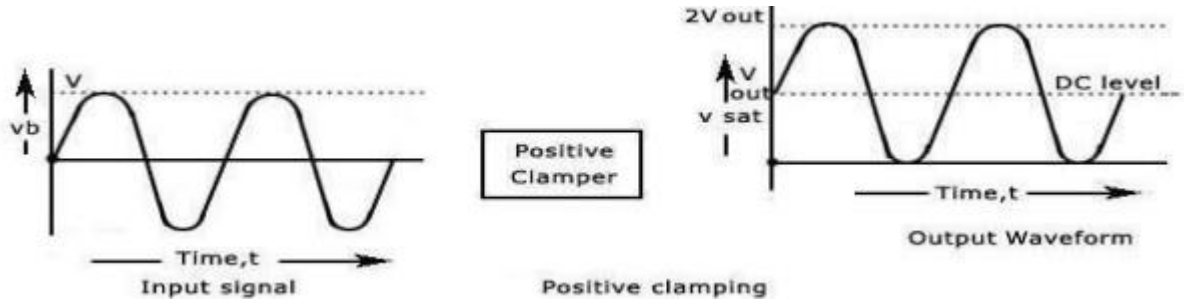
COMBINATION CLIPPER:- Combination clipper is employed when a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed) using a biased positive and negative clipper together. The circuit for such a clipper is given in the figure below.



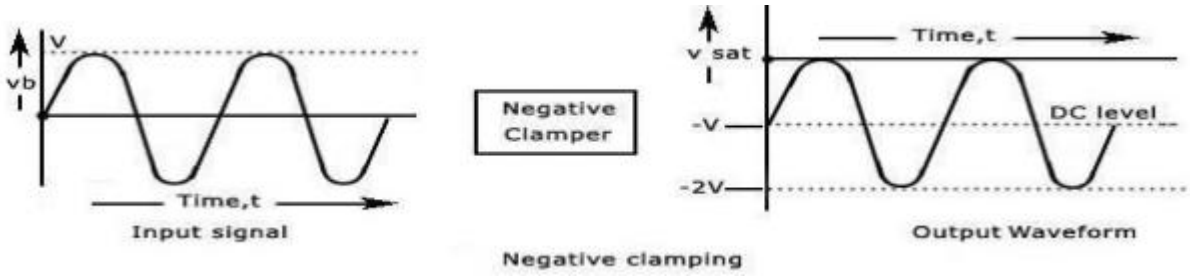
For positive input voltage signal when input voltage exceeds battery voltage +V1 diode D1 conducts heavily while diode D2 is reversed biased and so voltage +V1 appears across the output. This output voltage +V1 stays as long as input signal voltage exceeds +V1. On the other hand for the negative input voltage signal, the diode D1 remains reverse biased and diode D2 conducts heavily only when input voltage exceeds battery voltage V2 in magnitude. Thus during the negative half cycle the output stays at -V2 so long as the input signal voltage is greater than -V2

CLAMPER CIRCUITS:-

A clamping circuit is used to place either the positive or negative peak of a signal at a desired level. The dc component is simply added or subtracted to/from the input signal. The clamper is also referred to as an IC restorer and ac signal level shifter. A clamp circuit adds the positive or negative dc component to the input signal so as to push it either on the positive side. The clamper is of two types :- 1. Positive clamper 2. Negative clamper The circuit will be called a positive clamper, when the signal is pushed upward side byt he circuit and the negative peak of the signal coincides with the zero level.



The circuit will be called a negative clamper, when the signal is pushed downward by the circuit and the¬ positive peak of the input signal coincides with the zero level.



For a clamping circuit at least three components — a diode, a capacitor and a resistor are required. Sometimes an independent dc supply is also required to cause an additional shift. The important points regarding clamping circuits are:

1. The shape of the waveform will be the same, but its level is shifted either upward or downward,

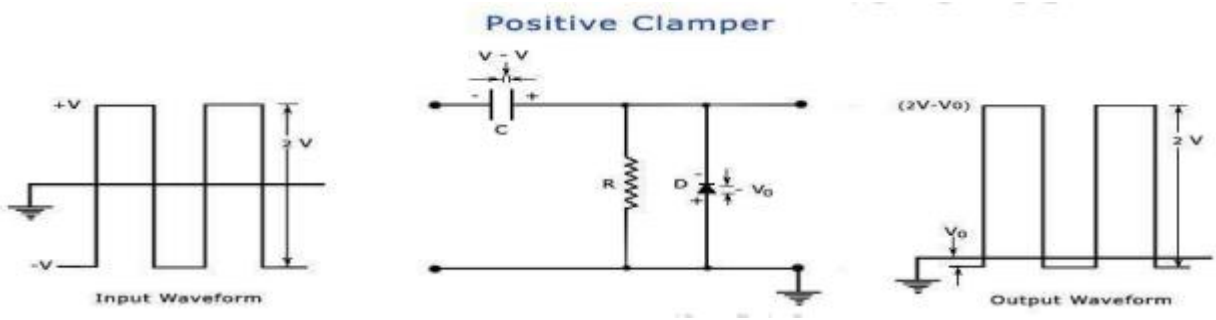
2. There will be no change in the peak-to-peak or r.m.s value of the waveform due to the clamping circuit. Thus, the input waveform and output waveform will have the same peak-to-peak value that is, 2Vmax. This is shown in the figure above. It must also be noted that same readings will be obtained in the ac voltmeter for the input voltage and the clamped output voltage.

3. There will be a change in the peak and average values of the waveform. In the figure shown above, the input waveform has a peak value of Vmax and average value over a complete cycle is zero. The clamped output varies from 2 Vmax and 0 (or 0 and -2Vmax). Thus the peak value of the clamped output is 2Vmax and average value is Vmax.

4. The values of the resistor R and capacitor C affect the waveform.

5. The values for the resistor R and capacitor C should be determined from the time constant equation of the circuit, t = RC. The values must be large enough to make sure that the voltage across capacitor C does not change significantly during the time interval the diode is non-conducting. In a good clamper circuit, the circuit time constant t = RC should be at least ten times the time period of the input signal voltage. It is advantageous to first consider the condition under which the diode becomes forward biased.

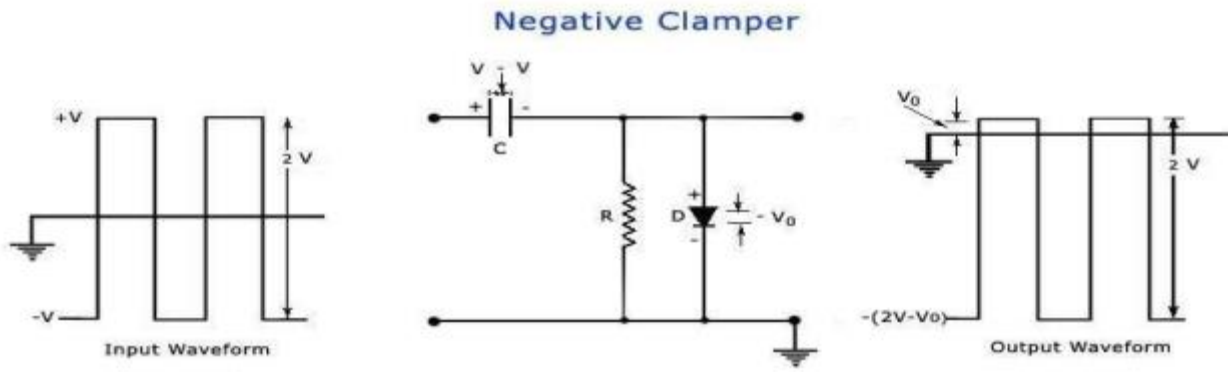
POSITIVE CLAMPER:- Consider a negative clamping circuit, a circuit that shifts the original signal in a vertical downward direction



The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the negative half cycle of input, the output voltage will be equal to the barrier potential of the diode, V0 and capacitor is charged to (V – V0). During the positive half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the positive portion of the input waveform. Thus during positive input, the output voltage will be the sum of the input voltage and capacitor voltage = +V + (V — V0) = +(2 V – V0) . The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to (2V-V0) - V0 = 2 V.

NEGATIVE CLAMPER:-

Consider a negative clamping circuit, a circuit that shifts the original signal in a vertical downward direction.

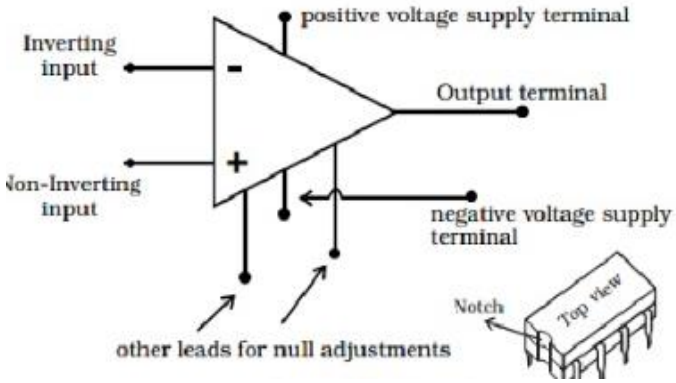


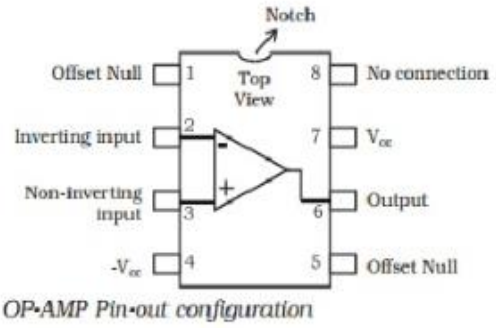
The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrier potential of the diode, V0 and capacitor is charged to (V – V0). During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus,¬ there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus during negative input, the output voltage will be the sum of the input voltage and capacitor voltage = – V – (V — V0) = – (2 V – V0) . The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to V0 - [-(2V-V0)] = 2 V.

UNIT VI OPERATIONAL AMPLIFIERS:

OPERATIONAL AMPLIFIER (OPAMP)

Operational Amplifier, also called as an Op-Amp, is an integrated circuit, which can be used to perform various linear, non-linear, and mathematical operations. An op-amp is a **direct coupled high gain amplifier**.





OP-AMP Pin-out configuration

The OP - AMP is represented by a triangular symbol as shown in Fig. It has two input terminals and one output terminal. The terminal with *negative* sign is called as the inverting input and the terminal with *positive* sign is called as the non-inverting input. The input terminals are at the base of the triangle. The output terminal is shown at the apex of the triangle.

The widely used very popular type of Op-Amp is IC 741. Referring to the top view of the dual-in-package, the pin configuration of IC 741 can be described (Fig) as follows. The top pin on the left side of the notch indicates Pin 1. The pin number 2 is inverting input terminal and 3 is non-inverting input terminal. Pin 6 is the output terminal. A d.c. voltage or a.c signal placed on the inverting input will be 180^o out of phase at the output. A d.c. voltage or a.c. signal placed on the non-inverting input will be inphase at the output. Pins 7 and 4 are the power supply terminals. Terminals 1 and 5 are used for null adjustment. Null adjustment pins are used to null the output voltage when equal voltages are applied to the input terminals for perfect balance. Pin 8 indicates no connection.

Ideal OPAMP and Practical OPAMP:

An ideal op-amp is a theoretical concept with infinite gain, infinite input impedance, zero output impedance, and infinite bandwidth, while a practical op-amp has limitations in these areas, such as finite gain, input impedance, output impedance, and bandwidth.

Ideal Op-Amp Characteristics:

- **Infinite Open-Loop Gain:** The output voltage changes infinitely for any input voltage difference.
- **Infinite Input Impedance:** No current is drawn from the input source, meaning the input impedance is infinitely large.
- **Zero Output Impedance:** The output voltage remains constant regardless of the load connected to the output, implying zero output impedance.

- **Infinite Bandwidth:** The op-amp can amplify signals of any frequency without distortion, meaning an infinite bandwidth.
- **Zero Input Offset Voltage:** The output voltage is zero when the input voltage is zero, meaning zero offset voltage.
- **Zero Input Bias Current:** No current flows into the input terminals.
- **Infinite Slew Rate:** The output voltage can change instantaneously, implying an infinite slew rate.
- **No Power Consumption:** The ideal op-amp consumes no power.
- **Zero Noise:** The op-amp does not introduce any noise.

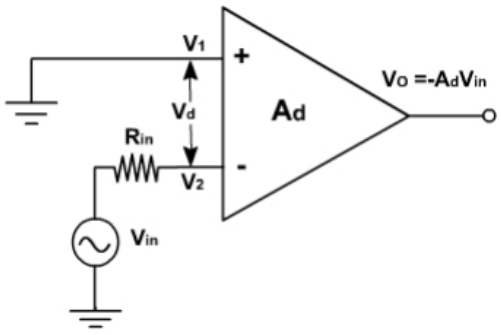
Practical Op-Amp Characteristics :

- **Finite Open-Loop Gain:** The op-amp has a limited gain, which typically decreases with increasing frequency.
- **Finite Input Impedance:** The op-amp draws a small amount of current from the input source, resulting in a finite input impedance.
- **Non-Zero Output Impedance:** The output voltage changes slightly when a load is connected, indicating a non-zero output impedance.
- **Finite Bandwidth:** The op-amp's gain drops at higher frequencies, limiting its bandwidth.
- **Non-Zero Input Offset Voltage:** There is a small voltage difference between the input terminals, even when the output is zero, resulting in a non-zero offset voltage.
- **Non-Zero Input Bias Current:** A small amount of current flows into the input terminals.
- **Finite Slew Rate:** The output voltage cannot change instantaneously, implying a finite slew rate.
- **Power Consumption:** The op-amp consumes power from the power supply.
- **Noise:** The op-amp introduces some noise, which can affect the output signal.

Slew Rate

At high signal speeds, there is a limit on the maximum rate of change of the amplifier output voltage. This limiting rate of change is called the **slew rate** (or **slewing rate**). It is usually expressed as volts per microsecond.

Virtual Ground Concept:



For an ideal OPAM open loop gain $A = \frac{V_o}{V_d}$

For an ideal OPAMP $A = \infty$

$$\Rightarrow \frac{V_o}{V_d} = \infty$$

$$\Rightarrow V_d = 0$$

$$\Rightarrow V_1 - V_2 = 0$$

$$\Rightarrow V_1 = V_2$$

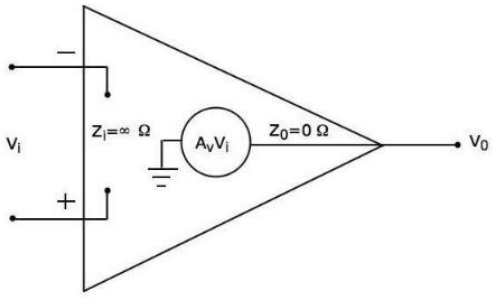
Hence when non-inverting terminal is grounded the inverting terminal will be virtually grounded.

This concept is called virtual ground concept. It is only applicable for ideal OPAMP.

OPAMP EQUIVALENT CIRCUIT:

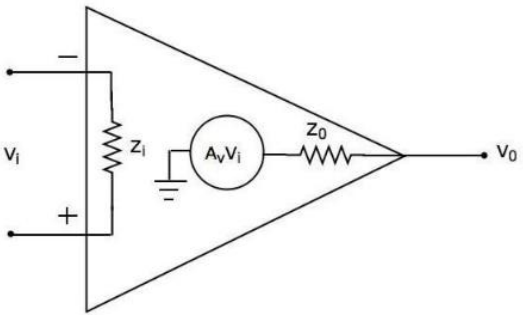
An ideal op-amp exists only in theory, and does not exist practically. The **equivalent circuit** of an ideal op-amp is shown in the figure given below −

Ideal Op-Amp



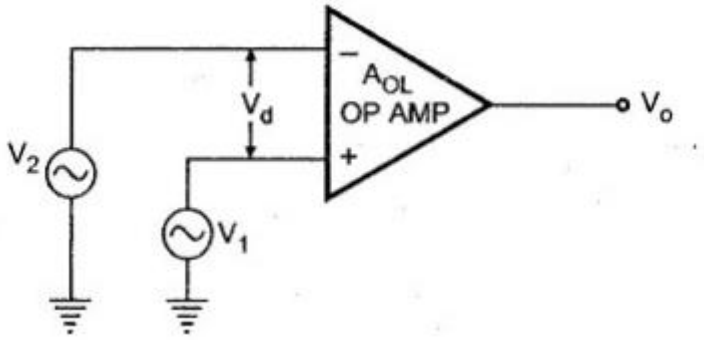
Practical Op-Amp

Practically, op-amps are not ideal and deviate from their ideal characteristics because of some imperfections during manufacturing. The **equivalent circuit** of a practical op-amp is shown in the following figure −



Open loop and closed loop configurations:

Open-Loop Configuration:



Open Loop Configuration of Op amp – The simplest possible way to use an opamp is in the open loop mode. Since the gain is very large in open loop condition the output voltage Vo is either at its positive saturation voltage +Vsat or –ive saturation voltage –Vsat as V1>V2 or V2>V1 Respectively.

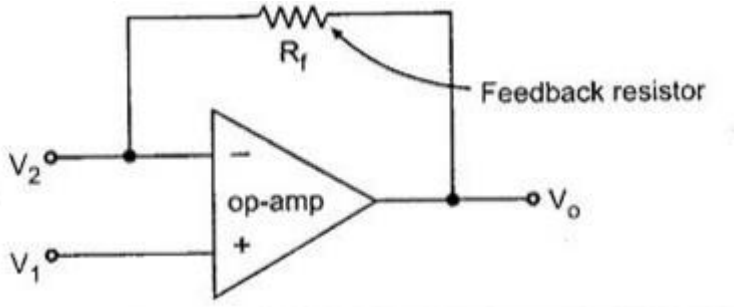
Features of Open-Loop Configuration:

- **No Feedback**: An open-loop op-amp configuration has no feedback path from the output back to the input.
- **High Gain**: The gain of an op-amp in open-loop configuration is very high, typically ranging from 100,000 to 1,000,000.
- **Instability:** The high gain makes the open-loop configuration unstable, and it is prone to oscillations and saturation.
- **Limited Applications:** Due to its instability, open-loop op-amp configurations are primarily used as comparators, where the output switches between two states based on the input voltage.
- **Example:** A simple open-loop configuration is a comparator circuit, where the output is either high or low depending on whether the input voltage is above or below a reference voltage.

Closed-Loop Configuration:

The Closed Loop Configuration of Op amp is possible using feedback. The feedback allows to feed some part of the output back to the input. In linear applications the op-amp is always used with negative feedback. The feedback helps to control gain which otherwise drives op-amp into saturation.

The gain resulting with feedback is called **closed loop gain** of the op-amp. Due to feedback resistance there is reduction in the gain.



Features of Closed-Loop Configuration:

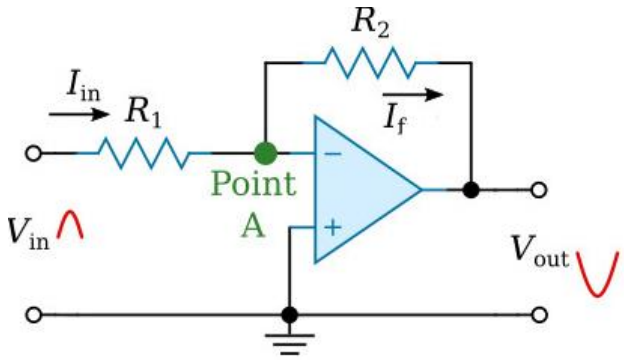
- **Feedback:** A closed-loop op-amp configuration uses a feedback path from the output back to the input, typically to the inverting input.
- **Stable Gain**: The feedback loop stabilizes the gain, making it predictable and controllable.
- **Reduced Gain**: The closed-loop gain is typically lower than the open-loop gain, but the reduced gain is offset by the increased stability and predictability.
- **Versatile Applications**: Closed-loop configurations are used for various applications, including amplification, filtering, and summing.
- **Example:** An inverting amplifier, non-inverting amplifier, and integrator are examples of closed-loop op-amp configurations.

UNIT-VII

APPLICATION OF OPAMP, TIMER CIRCUITS & IC VOLTAGE REGULATOR

1) OPAMP as Inverting Amplifier:

When the input is given through inverting terminal and non-inverting terminal is grounded the OPAMP is said to be operating in inverting mode.



Applying KCL at point 'A'

$$I_i = I_f$$

$$\Rightarrow \frac{V_{in} - V_A}{R_1} = \frac{V_A - V_{out}}{R_2}$$

$$\Rightarrow \frac{V_{in}}{R_1} = \frac{-V_{out}}{R_2}$$

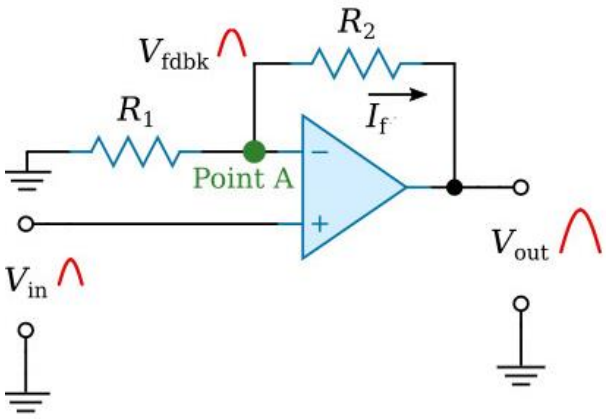
[Due to Virtual ground V_A =0]

$$\Rightarrow V_{out} = \frac{-R_2}{R_1} V_{in} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (i)$$

Eq(i) is the output of Inverting OPAMP in closed loop configuration.

2) OPAMP as Non-inverting Amplifier:

When the input is given through non-inverting terminal and inverting terminal is grounded the OPAMP is said to be operating in non-inverting mode.



Applying KCL at point 'A'

$$I_i = I_f$$

$$\Rightarrow \frac{0 - V_A}{R_1} = \frac{V_A - V_{out}}{R_2}$$

$$\Rightarrow \frac{-V_{in}}{R_1} = \frac{V_{in} - V_{out}}{R_2}$$

$$\Rightarrow \frac{-V_{in}}{R_1} = \frac{V_{in}}{R_2} - \frac{V_{out}}{R_2}$$

[Due to Virtual ground V_A =V_i]

$$\Rightarrow \frac{V_o}{R_2} = \frac{V_{in}}{R_2} + \frac{V_{in}}{R_1} = V_{in}\left(\frac{1}{R_2} + \frac{1}{R_1}\right)$$

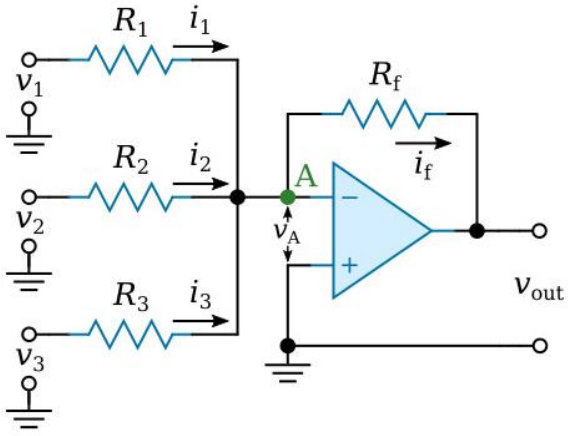
$$\Rightarrow V_o = V_i\left(1 + \frac{R_2}{R_1}\right) \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (ii)$$

Eq(ii) is the output of Non-Inverting OPAMP in closed loop configuration.

3) OPAMP as an ADDER:

An adder is an electronic circuit that produces an output, which is equal to the sum of the applied inputs.

An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal.



Applying KCL at point 'A'

$$\boldsymbol{i_1 + i_2 + i_3 = i_f}$$

$$\boldsymbol{\Rightarrow \frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_{out}}{R_f}}$$

$$\boldsymbol{\Rightarrow \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3} = \frac{0 - V_{out}}{R_f}}$$

[Due to Virtual ground V_A =0]

$$\boldsymbol{\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_{out}}{R_f}}$$

$$\boldsymbol{\Rightarrow V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}$$

$$\textbf{If } \boldsymbol{R_1 = R_2 = R_3 = R}$$

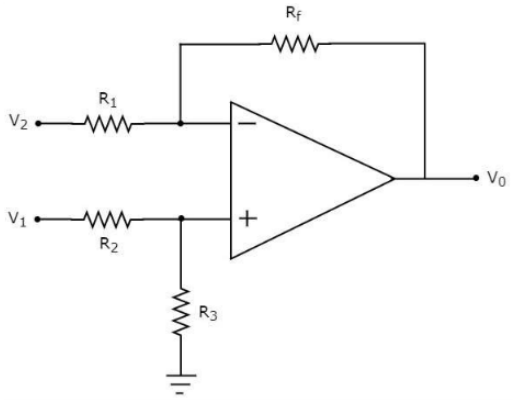
$$\textbf{Then } \boldsymbol{\Rightarrow V_{out} = \frac{-R_f}{R}(V_1 + V_2 + V_3)}$$

4) OPAMP as a SUBSTRACTOR

A subtractor is an electronic circuit that produces an output, which is equal to the difference of the applied inputs. This section discusses about the op-amp based subtractor circuit.

An op-amp based subtractor produces an output equal to the difference of the input voltages applied at its inverting and non-inverting terminals. It is also called as a difference amplifier, since the output is an amplified one.

The circuit diagram of an op-amp based subtractor is shown in the following figure –

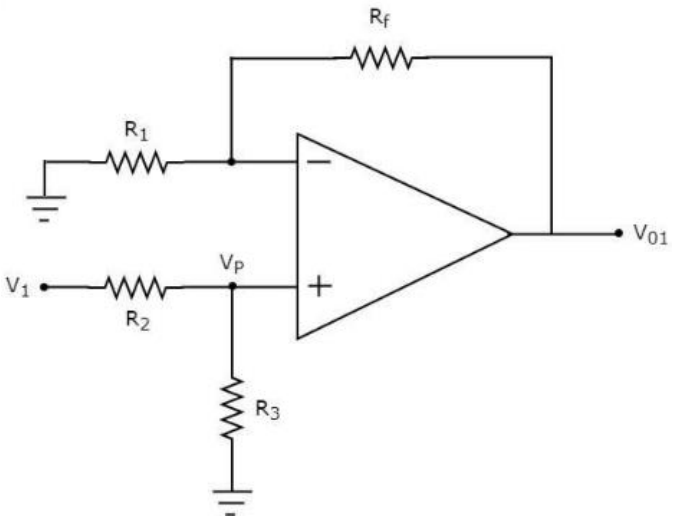


Now, let us find the expression for output voltage V0V0 of the above circuit using superposition theorem using the following steps −

Step 1

Firstly, let us calculate the output voltage V_{01} by considering only V_1.

For this, eliminate V_2 by making it short circuit. Then we obtain the modified circuit diagram as shown in the following figure –



Now, using the voltage division principle, calculate the voltage at the non-inverting input terminal of the op-amp.

$$=> V_p = V_1\left(\frac{R_3}{R_2+R_3}\right)$$

Now, the above circuit looks like a non-inverting amplifier having input voltage Vp. Therefore, the output voltage V_{01} of above circuit will be

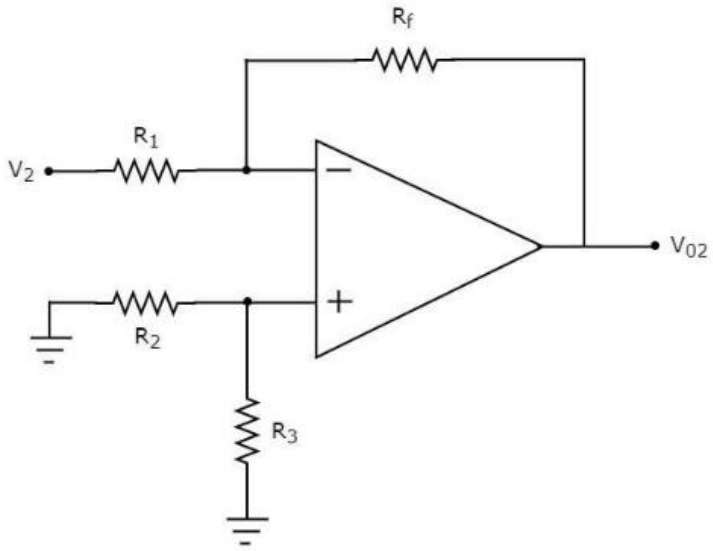
$$V_{01} = V_p\left(1+\frac{R_f}{R_1}\right)$$

Substitute, the value of Vp in above equation, we obtain the output voltage V_{01} by considering only V_1, as –

$$V_{01} = V_1 \left(\frac{R_3}{R_2 + R_3} \right) \left(1 + \frac{R_f}{R_1} \right)$$

Step 2

In this step, let us find the output voltage, V02V02 by considering only V2V2. Similar to that in the above step, eliminate V1V1 by making it short circuit. The **modified circuit diagram** is shown in the following figure.



You can observe that the voltage at the non-inverting input terminal of the op-amp will be zero volts. It means, the above circuit is simply an **inverting op-amp**. Therefore, the output voltage V_{02} of above circuit will be −

$$V_{02} = \left(-\frac{R_f}{R_1} \right) V_2$$

Step 3

In this step, we will obtain the output voltage V_0 of the subtractor circuit by adding the output voltages obtained in Step1 and Step2. Mathematically, it can be written as:

$$V_0 = V_{01} + V_{02}$$

Substituting the values of V_{01} and V_{02} in the above equation, we get –

$$V_0 = V_1\left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right)+\left(-\frac{R_f}{R_1}\right)V_2$$

$$=> V_0 = V_1\left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right)-\left(\frac{R_f}{R_1}\right)V_2$$

If Rf=R1=R2=R3=R, then the output voltage V_0 will be

$$V_0 = V_1\left(\frac{R}{R+R}\right)\left(1+\frac{R}{R}\right)-\left(\frac{R}{R}\right)V_2$$

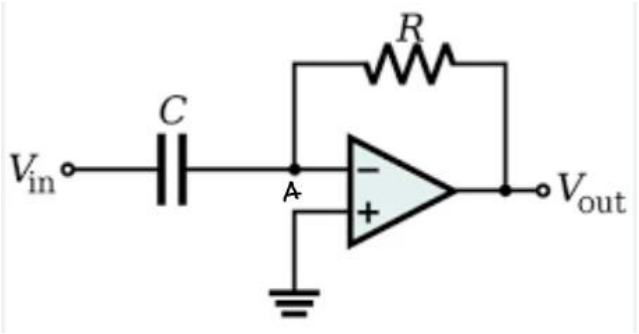
$$=> V_0 = V_1\left(\frac{R}{2R}\right)(2)-(1)V_2$$

$$V_0 = V_1 - V_2$$

Thus, the op-amp based subtractor circuit discussed above will produce an output, which is the difference of two input voltages V_1 and V_2, when all the resistors present in the circuit are of same value.

5) OPAMP as a Differentiator:

A differentiator is an electronic circuit that produces an output equal to the first derivative of its input.



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to the virtual short concept, the voltage at the inverting input terminal of opamp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The nodal equation at the inverting input terminal's node is −

$$C\frac{\mathrm{d}(0-V_i)}{\mathrm{d}t}+\frac{0-V_0}{R}=0$$

$$=>-C\frac{\mathrm{d}V_i}{\mathrm{d}t}=\frac{V_0}{R}$$

$$=>V_0=-RC\frac{\mathrm{d}V_i}{\mathrm{d}t}$$

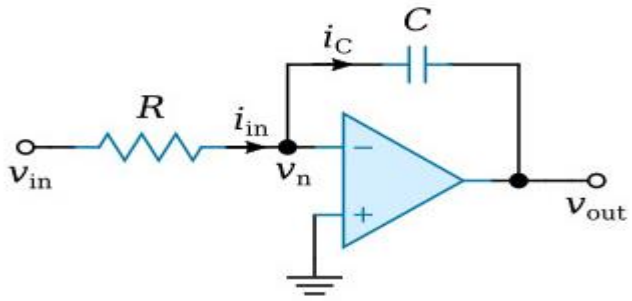
If $RC=1\,\text{sec}$, then the output voltage V_0 will be −

$$V_0=-\frac{\mathrm{d}V_i}{\mathrm{d}t}$$

Thus, the op-amp based differentiator circuit shown above will produce an output, which is the differential of input voltage Vi, when the magnitudes of impedances of resistor and capacitor are reciprocal to each other.

6) OPAMP as an Integrator

The figure below shows an integrator. The capacitor of this circuit connects the inverting input and the output signal points of the operational amplifier in such a manner that the output potential varies as the time integral of the input potential.



Applying KCL at V_n

$$i_{in}=i_c$$

$$\frac{V_{in}-V_n}{R}=C\frac{d}{dt}(V_n-V_o)$$

According to Virtual ground concept

$$V_n=0$$

Substituting this value in the equation

$$\Rightarrow\frac{V_{in}-0}{R}=C\frac{d}{dt}(0-V_o)$$

$$\Rightarrow\frac{V_{in}}{R}=C\frac{d}{dt}(-V_o)$$

$$\Rightarrow\frac{V_{in}}{R}=-C\frac{d}{dt}(V_o)$$

$$\Rightarrow dV_o = -\frac{1}{RC} V_{in} dt$$

Integrating both sides

$$\therefore V_o = -\frac{1}{RC} \int V_{in} dt$$

where $RC=T$ is the time constant of the integrator. This determines the amplitude scaling which is applied. The relation of the previous equation indicates that a voltage may be integrated with respect to time.

7) OPAMP as a COMPARATOR

A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser.

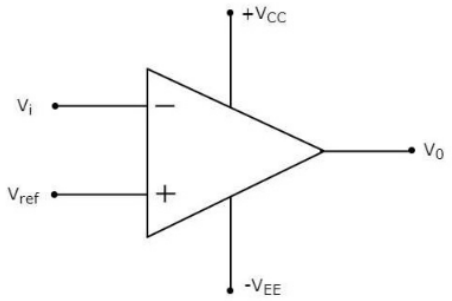
An op-amp consists of two input terminals and hence an op-amp based comparator compares the two inputs that are applied to it and produces the result of comparison as the output.

Comparators are of two types : **Inverting** and **Non-inverting**. This section discusses about these two types in detail.

Inverting Comparator

An **inverting comparator** is an op-amp based comparator for which a reference voltage is applied to its non-inverting terminal and the input voltage is applied to its inverting terminal. This comparator is called as **inverting** comparator because the input voltage, which has to be compared is applied to the inverting terminal of op-amp.

The **circuit diagram** of an inverting comparator is shown in the following figure.

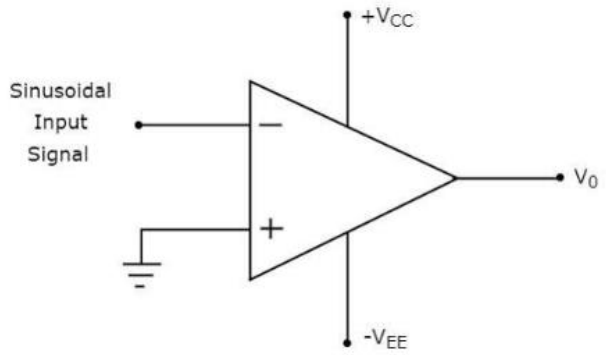


The **operation** of an inverting comparator is very simple. It produces one of the two values, +Vsat and −Vsat at the output based on the values of its input voltage Vi and the reference voltage Vref.

- The output value of an inverting comparator will be −Vsat, for which the input Vi voltage is greater than the reference voltage Vref.
- The output value of an inverting comparator will be +Vsat, for which the input Vi is less than the reference voltage Vref.

EXAMPLE:

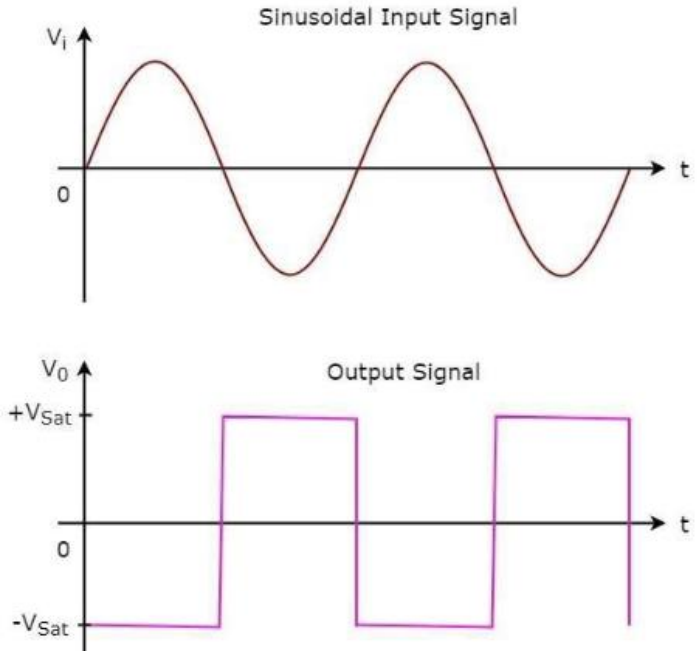
Let us draw the output wave form of an inverting comparator, when a sinusoidal input signal and a reference voltage of zero volts are applied to its inverting and non-inverting terminals respectively.



The **operation** of the inverting comparator shown above is discussed below −

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of op-amp is greater than zero volts. Hence, the output value of the inverting comparator will be equal to −Vsat during positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of the op-amp is less than zero volts. Hence, the output value of the inverting comparator will be equal to +Vsat during negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of an inverting comparator, when the reference voltage is zero volts.

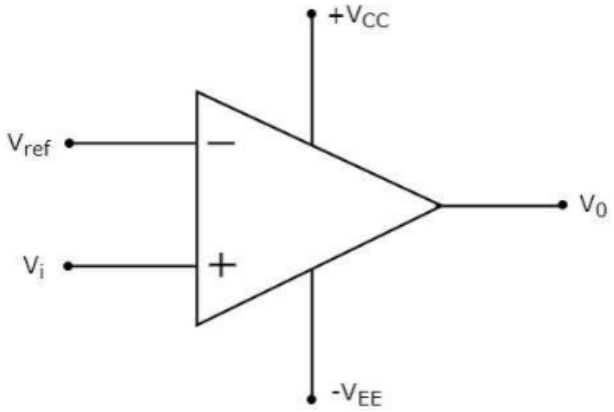


In the figure shown above, we can observe that the output transitions either from −Vsat to +Vsat or from +Vsat to −Vsat whenever the sinusoidal input signal is crossing zero volts. In other words, output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **inverting zero crossing detector.**

Non-Inverting Comparator

A non-inverting comparator is an op-amp based comparator for which a reference voltage is applied to its inverting terminal and the input voltage is applied to its non-inverting terminal. This op-amp based comparator is called as **non-inverting** comparator because the input voltage, which has to be compared is applied to the non-inverting terminal of the op-amp.

The **circuit diagram** of a non-inverting comparator is shown in the following figure

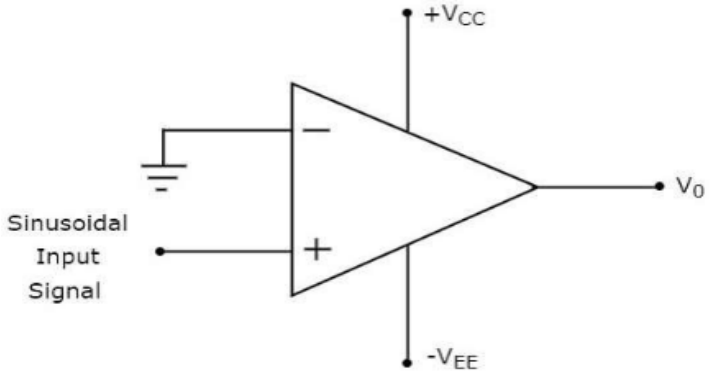


The **operation** of a non-inverting comparator is very simple. It produces one of the two values, +Vsat and −Vsat at the output based on the values of input voltage Vt and the reference voltage +Vref.

- The output value of a non-inverting comparator will be +Vsat, for which the input voltage Vi is greater than the reference voltage +Vref.
- The output value of a non-inverting comparator will be −Vsat, for which the input voltage Vi is less than the reference voltage +Vref.

Example

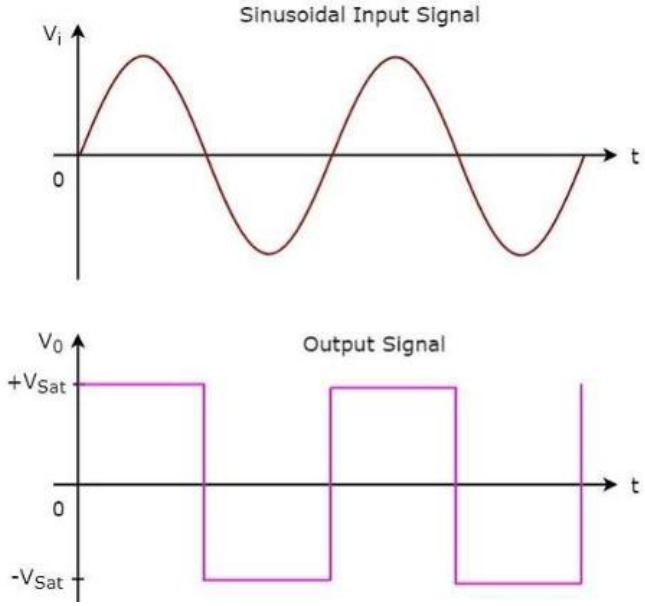
Let us draw the **output wave form** of a non-inverting comparator, when a sinusoidal input signal and reference voltage of zero volts are applied to the non-inverting and inverting terminals of the op-amp respectively.



The **operation** of a non-inverting comparator is explained below −

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is greater than zero volts. Hence, the output value of a non-inverting comparator will be equal to +Vsat during the positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is less than zero volts. Hence, the output value of non-inverting comparator will be equal to −Vsat during the negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of a non-inverting comparator, when the reference voltage is zero volts.



From the figure shown above, we can observe that the output transitions either from +Vsat to −Vsat or from −Vsat to +Vsat whenever the sinusoidal input signal crosses zero volts. That means, the output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **non-inverting zero crossing detector**.