

Academic Lesson Plan of Winter 2026

Department : CSE	Semester : 3rd	Name of the teaching faculty: SHIBANI MADHUSMITA SAHOO
Subject: DE&CO	No. of days/per week class allotted . 3p/week.	Semester from : 1ST July 2026
		No. of weeks:15 weeks
		Topics to be covered:
1 st week	1 st	Difference Between Analog and Digital Signals
	2 nd	Number Systems: Binary, Octal
	3 rd	Number Systems: Decimal, and Hexadecimal
2 nd week	1 st	Number Systems: Decimal, and Hexadecimal
	2 nd	Conversion Between Number Systems
	3 rd	Binary Arithmetic Boolean Algebra
3 rd week	1 st	Basic Operations, Laws, and Simplification
	2 nd	Revision
	3 rd	Logic Gates: AND, OR
4 th week	1 st	NOT, NAND, NOR
	2 nd	XOR, XNOR
	3 rd	Design and Simplification of Logic Circuits Using Boolean Algebra
5 th week	1 st	Design and Simplification of Logic Circuits Using Boolean Algebra
	2 nd	Karnaugh Maps (K-Maps) for Simplification
	3 rd	Practical Applications of Logic Gates in Real-World Circuits
6 th week	1 st	Revision
	2 nd	Combinational Circuits: Multiplexers, Demultiplexers
	3 rd	Encoders, and Decoders
7 th week	1 st	Sequential Circuits: Flip-Flops (SR, JK, D, T)
	2 nd	Sequential Circuits: Flip-Flops (SR, JK, D, T)
	3 rd	Synchronous and Asynchronous Counters
8 th week	1 st	Synchronous and Asynchronous Counters
	2 nd	Registers and Shift Registers: Types and Uses
	3 rd	Revision
9 th week	1 st	Basic Structure of a Computer: CPU, Memory, Input/Output Devices
	2 nd	Basic Structure of a Computer: CPU, Memory, Input/Output Devices
	3 rd	Instruction Cycle: Fetch, Decode
10 th week	1 st	Execute Memory Organization: Types of Memory
	2 nd	RAM, ROM, Cache, Virtual Memory
	3 rd	Introduction to Buses: Address Bus, Data Bus, and Control Bus
11 th week	1 st	Introduction to Buses: Address Bus, Data Bus, and Control Bus
	2 nd	Revision
	3 rd	Unit Introduction to Microprocessors and Microcontrollers
12 th week	1 st	Basics of Arithmetic Logic Unit (ALU) and Control Unit
	2 nd	Basics of Arithmetic Logic Unit (ALU) and Control Unit
	3 rd	Instruction Set Architecture (ISA): RISC vs CISC Pipelining
13 th week	1 st	Instruction Set Architecture (ISA): RISC vs CISC Pipelining
	2 nd	Performance Optimization in Processors
	3 rd	Revision
14 th week	1 st	I/O Devices and Interfaces: Keyboard, Mouse, Printers
	2 nd	Storage Devices Interrupts, DMA (Direct Memory Access)
	3 rd	Multicore Processors, GPUs, and Embedded Systems
15 th week	1 st	Design a Simple Digital Circuit or Simulate a Basic CPU Operation
	2 nd	Design a Simple Digital Circuit or Simulate a Basic CPU Operation
	3 rd	Revision

COURSE OUTCOMES

CO.1	Define the fundamental concepts of digital electronics, including number systems, Boolean algebra, and logic gates.
CO.2	Explain the working principles of combinational and sequential circuits such as multiplexers, flip-flops, and counters and their

CO.3	Implement simplified logic circuits using Karnaugh Maps and Boolean algebra for solving digital design problems.
CO.4	Analyze instruction cycles, memory organization, and processor architecture to evaluate system performance and identify
CO.5	Design and simulate basic CPU operations or functional digital circuits using digital electronics and computer organization

Shibane Madhusmita Sahoo

Signature of Faculty


HOD, CSE